1 Single Stage Amplifiers

In this Unit,

- Single stage amplifiers in the three configurations of C.E, C.B, C.C, with design aspects are given.
- Using the design formulae for A_V, A_I, R_i, R_o etc., the design of single stage amplifier circuits is to be studied.
- Single stage JFET amplifiers in C.D, C.S and C.G configurations are also given.
- The Hybrid - π equivalent circuit of BJT, expressions for Transistor conductances and capacitances are derived.
- Miller's theorem, definitions for f_β and f_T are also given.
- Numerical examples, with design emphasis are given.

Introduction

An electronic amplifier circuit is one, which modifies the characteristics of the input signal, when delivered the output side. The modification in the characteristics of the input signal can be with respect to voltage, current, power or phase. Any one or all these characteristics power, or phase may be changed by the amplifier circuit.

1.1 CLASSIFICATION OF AMPLIFIERS

Amplifier circuits are classified in different ways as indicated below :

Types of Classification is Based on

(a) Frequency range
(b) Type of coupling
(c) Power delivered/conduction angle
(d) Signal handled.

(a) Frequency Range

AF (Audio Freq.)	:	40 Hzs – 15/20 kHz
RF (Radio Freq.)	:	> 20 kHz
Video Frequency	:	5 – 8 MHz
VLF (Very Low Freq.)	:	10 – 30 kHz
LF (Low Frequency)	:	30 – 300 kHz
Medium Frequency	:	300 – 3000 kHz
High Frequency	:	3 – 30 MHz
VHF (Very High Freq.)	:	30 – 300 MHz
UHF (Ultra High Freq.)	:	300 – 3000 MHz
SHF (Super High Freq.)	:	3000 – 30,000 MHz

(b) Types of Coupling

1. Direct coupled
2. RC coupled
3. Transformer coupled
4. LC Tuned Amplifiers
5. Series fed.

(c) Output power delivered/conduction angle

1. Low power (tens of mW or less).
2. Medium power (hundreds of mW).
3. High power (Watts).

Class A	360°
Class B	180°
Class AB	180 – 360°
Class C	< 180°
Class D	Switching type.
Class S	Switching type.

(d) Type of signal handled

1. Large signal 2. Small signal

In addition to voltage amplification A_V, current amplification A_I or power amplification A_P is expected from an amplifier circuit. The amplifier circuit must also have other characteristics like High input impedance (Z_i or R_i), Low output impedance (Z_o or R_o), Large Band Width (BW), High signal to Noise Ratio (S/N), and large *Figure of Merit (Gain BW product).*

In order that the amplified signal is coupled to the load R_L or Z_L, for all frequencies of the input signal range, so that maximum power is transferred to the load, (the condition required for maximum power transfer is $|Z_0| = |Z_L|$ or $R_0 = R_L$) coupling the output of amplifier V_0 to load R_L or Z_L is important. When reactive elements are used in the amplifier circuit, and due to internal junction capacitances of the active device, the Z_i and Z_o of the amplifier circuit change with frequency. As the input signal frequency varies over a wide range, and for all these signals amplification and impedance matching have to be achieved, coupling of the output of the amplifier to the load is important.

Since the gain A_V, A_I or A_P that can be obtained from a single stage amplifier circuit where only one active device (BJT, JFET or MOSFET) is used, the amplifier circuits are cascaded to get large gain. Multistage amplifier circuits are discussed in the next chapter.

When the frequency of the input signal is high (greater than A.F. range) due to internal junction capacitances of the actual device, the equivalent circuit of the BJT used earlier is not valid. So another model of BJT valid for high frequencies, proposed by Giacoletto is studied in this chapter.

1.2 DISTORTION IN AMPLIFIERS

If the input signal is a sine wave the output should also be a true sine wave. But in all the cases it may not be so, which we characterize as distortion. Distortion can be due to the nonlinear characteristic of the device, due to operating point not being chosen properly, due to large signal swing of the input from the operating point or due to the reactive elements L and C in the circuit. Distortion is classified as :

(a) ***Amplitude distortion :*** This is also called non linear distortion or harmonic distortion. This type of distortion occurs in large signal amplifiers or power amplifiers. It is due to the nonlinearity of the characteristic of the device. This is due to the presence of new frequency signals which are not present in the input. If the input signal is of 10 KHz the output signal should also be 10 kHz signal. But some harmonic terms will also be present. Hence the amplitude of the signal (rms value) will be different $V_0 = A_V V_i$. But it will be V_0'.

(b) ***Frequency distortion :*** The amplification will not be the same for all frequencies. This is due to reactive component in the circuit.

(c) ***Phase-shift delay distortion :*** There will be phase shift between the input and the output and this phase shift will not be the same for all frequency signals. It also varies with the frequency of the input signal.

In the output signal, all these distortions may be present or any one may be present because of which the amplifier response will not be good.

Example : 1.1

The transistor parameters are given as,

$h_{ie} = 2$ k $\quad h_{fe} = 50 \quad h_{re} = 6 \times 10^{-4} \quad h_{oe} = 25$ μA/V

$h_{ic} = 2$ k $\quad h_{fc} = -51 \quad h_{rc} = 1 \quad h_{oc} = 25$ μA/V

Find the individual as well as overall voltage gains and current gains. (Fig. 1.1(a)).

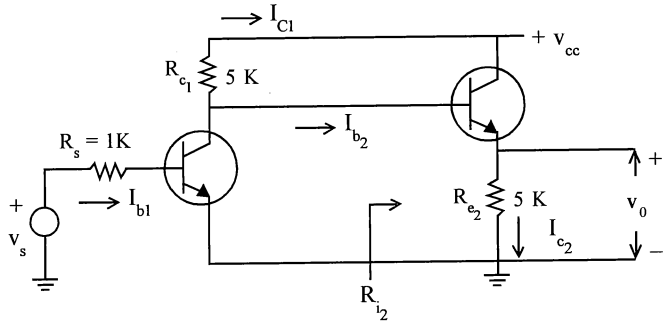

Fig. 1.1 (a) Circuit for Ex : 1.1

Solution :

It is advantageous to start the analysis with the last stage. Compute the current gain first, then the input impedance and voltage gain.

II stage : For the second stage $R_L = R_{e_2}$

$$A_{I_2} = \frac{-I_{e2}}{I_{b2}} = \frac{-h_{fc}}{1+h_{oc}R_{e2}}$$

$$= \frac{51}{1+25\times10^{-6}\times5\times10^{3}}$$

$$= \mathbf{45.3}$$

Input impedance $R_{i_2} = h_{ic} + h_{rc}\ A_{I_2}\ R_{e_2}$

$= 2 + 45.3 \times 5\text{k} = 228.5$ k.

$\therefore$ Input Z of the C.C. stage is very high.

Voltage gain of the second stage

$$A_{V_2} = \frac{V_0}{V_2} = A_{I_2}\ \frac{R_{e2}}{R_{i_2}}$$

$\because$ $V_0 = I_{e_2}\ R_{e_2}$;

V_2 = Input voltage for the second stage = $R_{i_2}\ .\ I_i$

$\therefore$ $$\frac{V_0}{V_2} = \frac{I_0 . R_{e2}}{I_i . R_{i_2}}$$

$$= A_{I_2} \frac{R_{e_2}}{R_{i_2}}$$

$$= \frac{45.3 \times 5}{228.5} = \mathbf{0.99}$$

I stage : For the first stage, the net load resistance in the parallel combination of R_{C_1} and R_{i_2} or

$$R_{i_2} = \frac{R_{c_1} . R_{i_2}}{R_{c_1} + R_{i_2}} = \frac{5 \times 228.5}{233.5} = 4.9 \text{ k}\Omega$$

Hence $$A_{I_1} = \frac{-I_{C_1}}{I_{b_1}} = \frac{-h_{fe}}{1 + h_{oe} R_{L_1}} = \frac{-50}{1 + 25 \times 10^{-6} \times 4.9 \times 10^3} = -44.5$$

The input impedance of the first stage will also be the input Z of the two stages since input Z of the second stage is also considered in determining the value of R_{L_1}. R_{i_1} depends on R_{L_1}.

$\therefore$ $$R_{i_1} = h_{i_e} + h_{r_e} A_{I_1} R_{L_1} \quad \text{(from the standard formula)}$$
$$= 2 - 6 \times 10^{-4} \times 44.5 \times 4.9$$
$$R_{i_1} = 1.87 \text{ k}\Omega.$$

Voltage gain of the first stage is,

$$A_{V_1} = \frac{V_2}{V_1} = \frac{A_{I_1} . R_{L_1}}{R_{i_1}}$$

$$= \frac{-44.5 \times 4.9}{1.87} = -116.6$$

$$A_I = \frac{-I_{e_2}}{I_{b_1}} = \frac{-I_{e_2}}{I_{b_2}} . \frac{+I_{b_2}}{I_{c_1}} . \frac{+I_{c_1}}{I_{b_1}}$$

$$= -A_{I_2} . \frac{I_{b_2}}{I_{c_1}} . A_{I_1}$$

In the actual circuit, the current gets branched into I_{c1} and I_{b2} which depend upon the values of R_{C_1} and R_{i_2}. (Fig. 1.1(b)).

$\because$ $$(-I_{b2} + I_{c1}) R_{c1} = I_{b2} . R_{i2}$$

$\therefore$ $$+ I_{b2} (R_{i2} + R_{c1}) = I_{c1} . R_{c1}$$

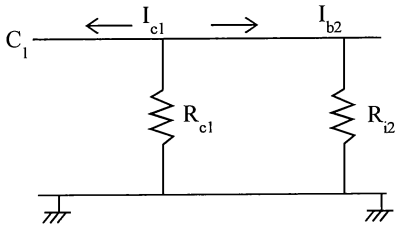

Fig. 1.1 (b) Current branching

$$\frac{I_{b2}}{I_{c1}} = \frac{R_{c1}}{R_{c1}+R_{i2}}$$

$$\therefore \quad A_I = A_{I2}\, A_{I1} \cdot \frac{R_{c1}}{R_{i2}+R_{c_1}}$$

$$= \frac{45.3\times(-44.5)\times 5}{228.5+5}$$

$$A_I = -43.2$$

$$A_V = \frac{V_0}{V_1} = \frac{V_0}{V_2} \cdot \frac{V_2}{V_1} = A_{V2} \cdot A_{V1}$$

$$A_V = 0.99 \times (-116.6) = -115.$$

$$\frac{I_{b2}}{I_{c1}} = \frac{R_{c1}}{R_{c1}+R_{i2}}$$

1.3 ANALYSIS OF CE, CC AND CB AMPLIFIERS

Small Signal Analysis means, we assume that the input AC signal peak to peak to amplitude is very small around the operating point Q as shown in Fig. 1.2. The swing of the signal always lies in the active region, and so the output is not distorted. In the *Large Signal Analysis,* the swing of the input signal is over a wide range around the operating point. The magnitude of the input signal is very large. Because of this the operating region will extend into the cutoff region and also saturation region.

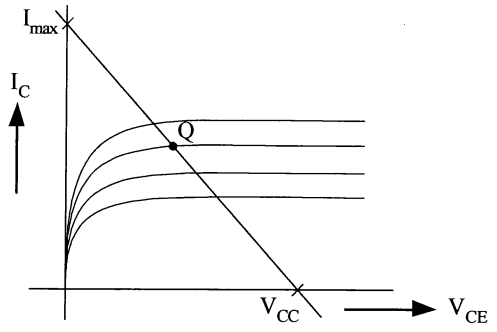

Fig. 1.2 Output characteristics of BJT

1.3.1 COMMON EMITTER AMPLIFIER

Common Emitter Circuit is as shown in the Fig. 1.3. The DC supply, biasing resistors and coupling capacitors are not shown since we are performing an *AC analysis*.

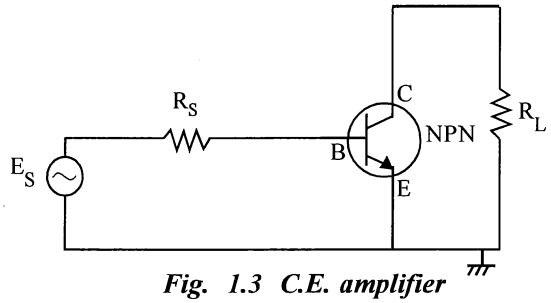

Fig. 1.3 C.E. amplifier

E_S is the input signal source and R_S is its resistance. The *h-parameter* equivalent for the above circuit is as shown in Fig. 1.4.

$$h_{ie} = \left.\frac{V_{be}}{I_b}\right|_{V_{ce}=0} \qquad h_{re} = \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0}$$

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b=0} \qquad h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0}$$

The typical values of the *h-parameter* for a transistor in Common Emitter Configuration are,

h_{ie} = 4 kΩ,

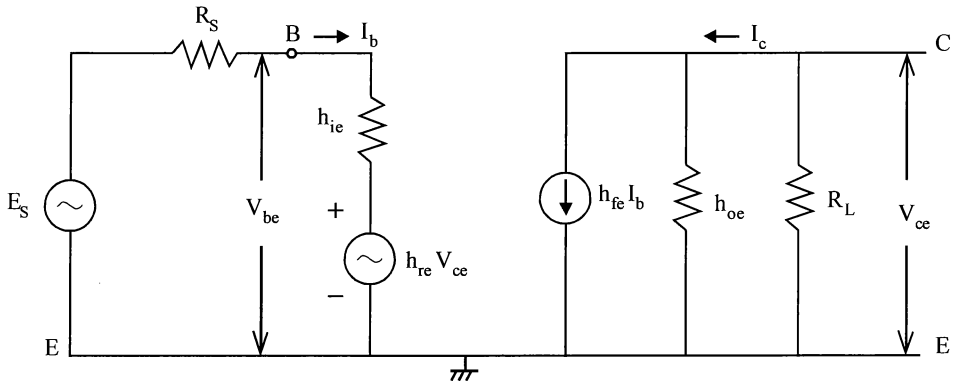

Fig. 1.4 h-parameter equivalent circuit

Since, $$h_{ie} = \frac{V_{be}}{I_b}$$

V_{be} is a fraction of volt 0.2V, I_b in μA, 100 μA and so on.

$$\therefore \qquad h_{ie} = \frac{0.2V}{50\times10^{-6}} = 4\ k\Omega$$

$$h_{fe} = I_c/I_b \simeq 100$$

I_C is in mA and I_B in μA.

$$\therefore \quad h_{fe} >> 1 \simeq \beta$$

$h_{re} = 0.2 \times 10^{-3}$. Because, it is the *Reverse* Voltage Gain.

$$h_{re} = \frac{V_{be}}{V_{ce}}$$

and $V_{ce} > V_{be}$;

$$h_{re} = \frac{\text{Input}}{\text{Output}}$$

Output is >> input, because amplification takes place. Therefore $h_{re} << 1$.

$$h_{oe} = 8\ \mu\text{℧} \quad \text{and} \quad h_{oe} = \frac{I_c}{V_{ce}}$$

1.3.2 Input Resistance of the Amplifier Circuit (R_i)

The general expression for R_i in the case of Common Emitter Transistor Circuit is

$$R_i = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe} + \frac{1}{R_L}} \qquad .....(1.1)$$

For Common Emitter Configuration,

$$R_i = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe} + \frac{1}{R_L}} \qquad .....(1.2)$$

R_i depends on R_L. If R_L is very small, $\frac{1}{R_L}$ is large, therefore the denominator in the second term is large or it can be neglected.

$$\therefore \quad R_i \cong h_{ie}$$

If R_L increases, the second term cannot be neglected.

$$R_i = h_{ie} - \text{(finite value)}$$

Therefore, R_i decreases as R_L increases. If R_L is very large, $\frac{1}{R_L}$ will be negligible compared to h_{oe}. Therefore, R_i remains constant. The graph showing R_i versus R_L is indicated in Fig. 1.5. R_i is not affected by R_L if $R_L < 1$ kΩ and $R_L > 1$ MΩ as shown in Fig. 1.5.

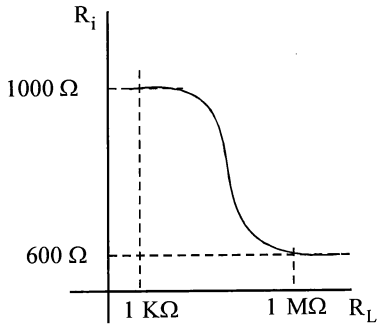

Fig. 1.5 Variation of R_i with R_L

R_i varies with frequency f because h-parameters will vary with frequency. h_{fe}, h_{re} will change with frequency f of the input signal.

1.3.3 Output Resistance of an Amplifier Circuit (R_0)

For Common Emitter Configuration,

$$R_o = \frac{1}{h_{oe} - \left(\frac{h_{re}h_{fe}}{h_{ie} + R_s}\right)} \qquad .....(1.3)$$

R_s is the resistance of the source. It is of the order of few hundred Ω.
R_0 depends on R_s. If R_s is very small compared to h_{ie},

$$R_o = \frac{1}{h_{oe} - \frac{h_{re}h_{fe}}{h_{ie}}} \quad (\text{independent of } R_s) \qquad .....(1.4)$$

Then, R_0 will be large of the order of few hundred kΩ. If R_s is very large, then

$$R_o \simeq \frac{1}{h_{oe}} \simeq 150 \text{ k}\Omega.$$

The graph is as shown in Fig. 1.6.

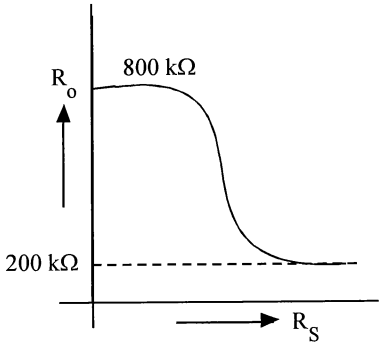

Fig. 1.6 Variation of R_o with R_S

1.3.4 Current Gain (A_i)

$$A_i = \frac{-h_{fe}}{1+h_{oe}R_L} \qquad .....(1.5)$$

If R_L is very small, $A_i \simeq h_{fe} \simeq 100$. So, Current Gain is large for Common Emitter Configuration. As R_L increases, A_i drops and when $R_L = \infty$, $A_i = 0$. Because, when $R_L = \infty$, output current I_0 or load current $I_L = 0$. Therefore, $A_i = 0$. Variation of A_i with R_L is shown in Fig. 1.7.

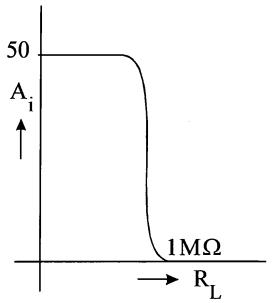

Fig 1.7 Variation of A_i with R_L

1.3.5 Voltage Gain (A_V)

$$A_V = \frac{-h_{fe}R_L}{h_{ie}+R_L(h_{ie}h_{oe}-h_{fe}h_{re})} \qquad .....(1.6)$$

If R_L is low, most of the output current flows through R_L. As R_L increases, output voltage increases and hence A_V increases. But if $R_L >> \frac{1}{h_{oe}}$, then the current from the current generator in the ***h-parameters*** equivalent circuit flows through h_{oe} and not R_L.

Then the, Output Voltage $= h_{fe} \cdot I_b \cdot \frac{1}{h_{oe}}$

(R_L is in parallel with h_{oe}. So voltage across h_{oe} = voltage across R_L). Therefore, V_0 remains constant as output voltage remains constant (Fig.1.8).

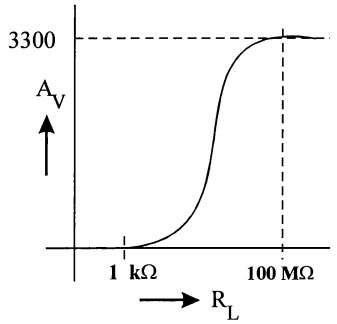

Fig. 1.8 Variation of A_v with R_L

1.3.6 Power Gain (A_p)

As R_L increases, A_I decreases. As R_L increases, A_V also increases.

Therefore, Power Gain which is the product of the two, A_V and A_I varies as shown in Fig. 1.9.

$$A_P = A_V A_I$$

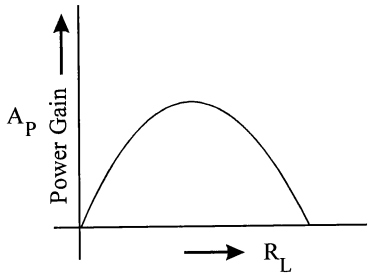

Fig. 1.9 Variation of A_P with R_L

Power Gain is maximum when R_L is in the range 100 kΩ – 1 MΩ i.e., when R_L is equal to the output resistance of the transistor. Maximum power will be delivered, under such conditions.

Therefore, it can be summarised as, Common Emitter Transistor Amplifier Circuit will have,

1. *Low to Moderate Input Resistance (300 Ω – 5 kΩ).*
2. *Moderately High Output Resistance (10 kΩ – 100 kΩ).*
3. *Large Current Amplification.*
4. *Large Voltage Amplification.*
5. *Large Power Gain.*
6. *180° phase-shift between input and output voltages.*

As the input current I_B, increases, I_C increases therefore drop across R_C increases and $V_0 = V_{CC} - V_I$ drop across R_C. Therefore, there is a phase shift of 180°.

The amplifier circuit is shown in Fig. 1.10.

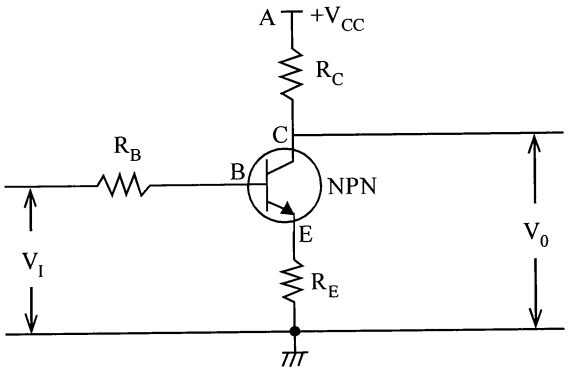

Fig. 1.10 CE amplifier circuit

1.3.7 Common Base Amplifier

The circuit diagram considering ***only AC*** is shown in Fig. 1.11.

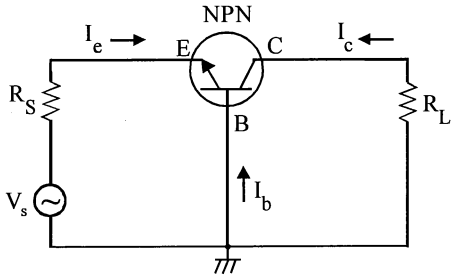

Fig. 1.11 CB amplifier

$$h_{ib} = \left.\frac{V_{eb}}{I_e}\right|_{V_{cb}=0}$$

V_{eb} is small fraction of a volt. I_e is in mA. So, h_{ib} is small.

$$h_{fb} = \left.\frac{I_c}{I_e}\right|_{V_{cb}=0} = -0.99 \text{ (Typical Value)}$$

$I_c < I_e \qquad \therefore \quad h_{fb} < 1$

$$h_{ob} = \left.\frac{I_c}{V_{cb}}\right|_{I_e=0} = 7.7 \times 10^{-8} \text{ mhos (Typical Value)}$$

I_c will be very small because $I_e = 0$. This current flows in between base and collector loop.

$$h_{rb} = \left.\frac{V_{eb}}{V_{cb}}\right|_{I_e=0} = 37 \times 10^{-6} \text{ (Typical Value)}$$

h_{rb} is small, because V_{eb} will be very small and V_{cb} is large.

1.3.8 Input Resistance (R_i)

$$R_i = h_{ib} - \frac{h_{fb}.h_{rb}}{h_{ob} + \frac{1}{R_L}}; \quad h_{fb} \text{ is -ve} \qquad \text{.....(1.7)}$$

when R_L is small < 100 kΩ, the second term can be neglected.

$\therefore \qquad R_i = h_{ib} \simeq 30\ \Omega.$

when R_L is very large, $\frac{1}{R_L}$ can be neglected.

$$R_i = h_{ib} - \frac{h_{fb}.h_{rb}}{h_{ob}}$$

So $R_i \simeq 500\ \Omega$ (Typical value) [$\because h_{fb}$ is negative]

$$\therefore \quad R_i = h_{ib} + \frac{h_{fb}h_{rb}}{h_{ob}}$$

The variation of R_i with R_L is shown in Fig. 1.12. R_i varies from 20 Ω to 500 Ω.

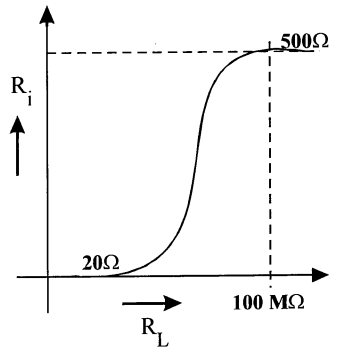

Fig. 1.12 Variation of R_i with R_L

1.3.9 Output Resistance (R_0)

$$R_o = \frac{1}{h_{ob} - \frac{h_{rb}h_{fb}}{h_{ib} + R_s}} \qquad \text{.....(1.8)}$$

If R_s is small, $R_o = 1 \Big/ \left(h_{ob} - \frac{h_{rb}h_{fb}}{h_{ib}} \right)$

But h_{fb} is negative.

$$\therefore \quad R_o = \frac{1}{h_{ob} + \frac{h_{rb}h_{fb}}{h_{ib}}}$$

This will be sufficiently large, of the order of 300 kΩ. Therefore, value of h_{ob} is small. As R_s increases, $R_o = \frac{1}{h_{ob}}$ also increases. [This will be much larger because, in the previous case, in the denominator, some quantity is subtracted from h_{ob}.]

$$\therefore \quad R_o = 12\ M\Omega$$

The variation of R_0 with R_s is shown in Fig. 1.13.

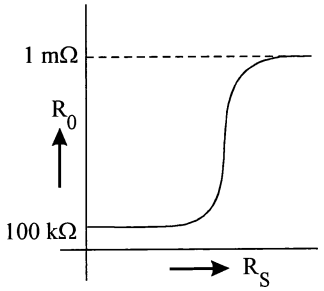

Fig. 1.13 Variation of R_0 with R_S

1.3.10 Current Gain (A_i)

$$A_i = \frac{-h_{fb}}{1+h_{ob}R_L} \qquad \text{.....(1.9)}$$

A_i is < 1. Because $h_{fe} < 1$. As R_L increases, A_i decreases. A_i is negative due to h_{fb}. The variation of A_i with R_L is shown in Fig. 1.14.

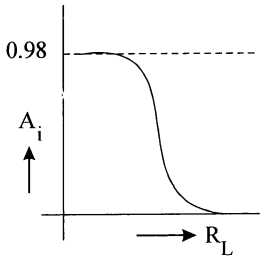

Fig. 1.14 Variation of A_i with R_L

1.3.11 Voltage Gain (A_v)

$$A_v = \frac{-h_{fb}R_L}{h_{ib}+R_L(h_{ib}h_{ob}-h_{fb}h_{rb})} \qquad \text{..... (1.10)}$$

As R_L increases, A_V also increases. If R_L tends to zero, A_V also tends to zero. ($A_V \rightarrow 0$, as $R_L \rightarrow 0$). The variation of Voltage Gain A_V with R_L is shown in Fig. 1.15.

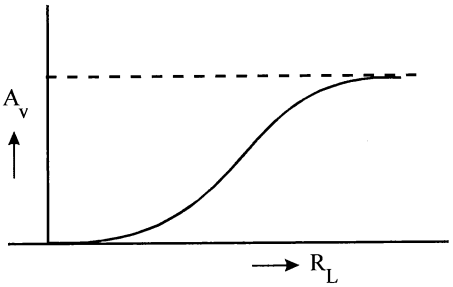

Fig. 1.15 Variation of A_v with R_L

1.3.12 POWER GAIN (A_P)

Power Gain $A_P = A_V \cdot A_I$

A_V increases as R_L increases. But A_I decreases as R_L increases. Therefore, Power Gain, which is product of both, varies with R_L as shown in Fig. 1.16.

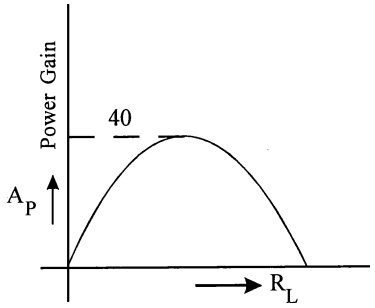

Fig 1.16 Variation of A_P with R_L

The characteristics of Common Base Amplifier with typical values are as given below.

1. *Low Input Resistance (few 100 Ω).*
2. *High Output Resistance (MΩ).*
3. *Current Amplification $A_i < 1$.*
4. *High Voltage Amplification and No Phase Inversion*
5. *Moderate Power Gain (30).* $\because$ $A_i < 1$.

1.3.13 COMMON COLLECTOR AMPLIFIER

The simplified circuit diagram for AC of a transistor (BJT) in Common Collector Configuration is as shown in Fig. 1.17 (without biasing resistors).

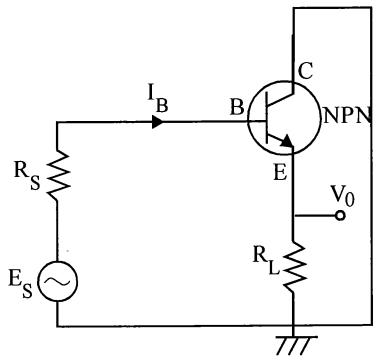

Fig. 1.17 CC Amplifier

The ***h-parameter*** equivalent circuit of transistor in Common Collector Configuration is shown in Fig. 1.18.

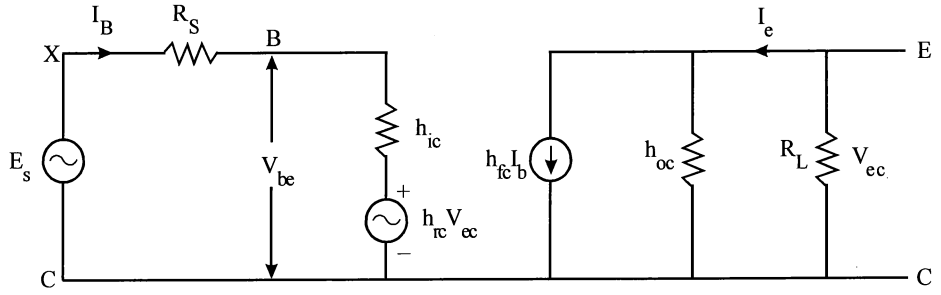

Fig. 1.18 h-parameter equivalent circuit

$$h_{ic} = \left.\frac{V_{bc}}{I_b}\right|_{V_{ec}=0} = 2{,}780\ \Omega \text{ (Typical Value)}$$

$$h_{oc} = \left.\frac{I_e}{V_{ec}}\right|_{I_b=0} = 7.7 \times 10^{-6} \text{ mhos (Typical Value)}$$

$$h_{fc} = -\left.\frac{I_e}{I_b}\right|_{V_{ce}=0} = 100 \text{ (Typical value)}$$

$\because\ I_e >> I_b$.

h_{fc} is negative because, I_E and I_B are in opposite direction.

$$h_{rc} = \left.\frac{V_{bc}}{V_{ec}}\right|_{I_b=0}; \quad V_{bc} = V_{ec} \text{ (Typical Value)}$$

Because, $I_B = 0$, E - B junction is not forward baised.

$\therefore\ V_{EB} = 0$.

For other circuit viz., Common Base and Common Emitter, h_r is much less than 1.

For Common Collector Configuration, $h_{rc} \simeq 1$.

The graphs (variation with R_C) are similar to Common Base Configuration.

Characteristics

1. *High Input Resistance $\simeq$ 3 kΩ (R_i)*
2. *Low Output Resistance 30 Ω (R_0)*
3. *Good Current Amplification $A_i >> 1$*
4. *$A_v \leq 1$*
5. *Lowest Power Gain of all the configurations.*

Since, A_v is < 1, the output voltage (Emitter Voltage) follows the input signal variation. Hence it is also known as *Emitter Follower*. The graphs of variation with R_L and R_S are similar to Common Base amplifier.

Example : 1.2

For the circuit shown in Fig.1.19 estimate A_i, A_v, R_i and R_o using reasonable approximations. The ***h-parameters*** for the transistor are given as

$h_{fe} = 100$ $h_{ie} = 2000\ \Omega$ h_{re} is negligible and $h_{oe} = 10^{-5}$ mhos(℧).

$I_b = 100\ \mu A$.

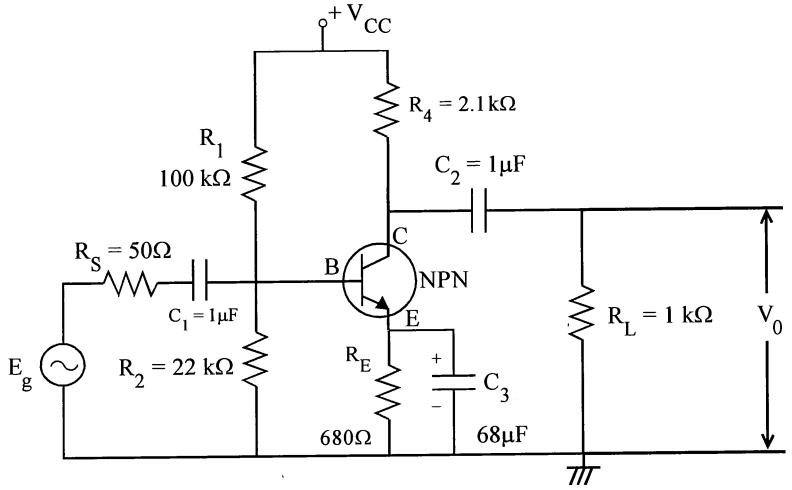

Fig. 1.19 CE amplifier circuit

Solution :

At the test frequency capacitive reactances can be neglected. V_{CC} point is at ground because the AC potential at $V_{CC} = 0$. So it is at ground. R_1 is connected between base and ground for AC. Therefore, $R_1 \parallel R_2$. R_4 is connected between collector and ground. So R_4 is in parallel with $1/h_{oe}$ in the output. The A.C. equivalent circuit in terms of ***h-parameters*** of the transistor is shown in Fig. 1.20.

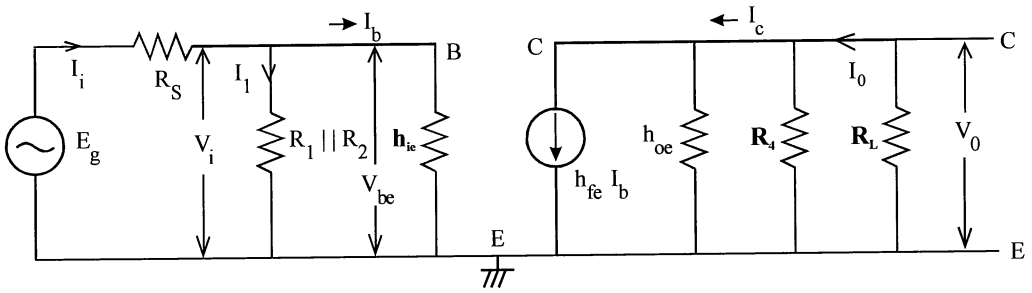

Fig. 1.20 Equivalent circuit

The voltage source $h_{re}\ V_{ce}$ is not shown since, h_{re} is negligible. At the test frequency of the input signal, the capacitors C_1 and C_2 can be regarded as short circuits. So they are not shown in the AC equivalent circuit. The emitter is at ground potential. Because X_{C_3} is also negligible, all the AC passes through C_3. Therefore, emitter is at ground potential and this circuit is in Common Emitter Configuration.

Input Resistance (R_i)

R_i input resistance looking into the base is h_{ie} only

The expression for R_i of the transistor alone $= h_{ie} - \left(\dfrac{h_{fe}\, h_{re}}{h_{oe} + \dfrac{1}{R_L}} \right)$.

R_L is very small and h_{re} is negligible. Therefore, the second term can be neglected. So R_i of the transistor alone is h_{ie}. Now R_i of the entire amplifier circuit, considering the bias resistors is,

$$R_i = h_{ie} \parallel R_1 \parallel R_2$$

$$\therefore \quad \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 22}{100 + 22} = 18\ \text{k}\Omega$$

$$\therefore \quad R_i = \frac{18 \times 2}{18 + 2} = 1.8\ \text{k}\Omega$$

Output Resistance (R_0)

$$R_0 = \frac{1}{h_{oe} - \left[\dfrac{h_{re} h_{fe}}{h_{ie} + R_S} \right]} \qquad \text{.....(1.11)}$$

Because, h_{re} is negligible, R_o of the transistor alone in terms of ***h-parameters*** of the transistor $= \dfrac{1}{h_{oe}}$. Now R_o of the entire amplifier circuit is,

$$\left(\frac{1}{h_{oe}} \parallel R_4 \parallel R_L \right) = (2.1 \times 10^{+3}) \parallel (100\ \text{k}\Omega) \parallel (1\ \text{k}\Omega)$$

$$= 2\ \text{k}\Omega. \parallel (1\ \text{k}\Omega) = 0.67\ \text{k}\Omega$$

Current Gain (A_i)

To determine A_i the direct formula for A_i in transistor in Common Emitter Configuration is, $\dfrac{-h_{fe}}{1 + h_{oe} R_L}$.

But this cannot be used because the input current I_i gets divided into I_1 and I_b. There is some current flowing through the parallel configuration of R_1 and R_2. So the above formula cannot be used.

$$V_{be} = I_b \cdot h_{ie}$$

$$V_{be} = 10^{-4} \times (2000) = 0.2\text{V}. \text{ (This is AC Voltage not DC)}$$

Voltage across R_1 R_2 parallel configuration is also V_{be}.

$$\therefore \quad \text{Current } I_1 = \frac{V_{be}}{50 \times 10^3} = \frac{0.2}{50\ \text{k}\Omega} = 4\ \mu\text{A}.$$

Therefore total input current,

$$I_i = I_1 + I_b = 4 + 100 = 104\ \mu A.$$

I_0 is the current through the 1 kΩ load.

$\frac{1}{h_{oe}}$ = 100 kΩ is very large compared with R_4 and R_L. Therefore, all the current on the output side, $h_{fe}\ I_b$ gets divided between R_4 and R_L only.

Therefore current through R_L is I_0,

$$I_0 = h_{fe}\ I_b \cdot \left[\frac{R_4}{R_4 + R_L}\right]$$

$$I_o = 100 \times 10^{-4}\ \frac{2.1\times10^3}{(2.1\times10^3 + 10^3)}$$

$$= 6.78\ \text{mA}.$$

Therefore current amplification,

$$A_i = \frac{I_0}{I_i}$$

$$= \frac{6.78\times10^{-3}}{104\times10^{-6}} = 65.$$

$$A_v = \frac{V_o}{V_i};\quad V_i = V_{be}$$

$$V_o = -\ I_0 \cdot R_L$$
$$= (-\ 6.78 \times 10^3) \times (10^3)$$
$$= -\ 6.78\text{V}$$

Because, the direction of I_0 is taken as entering into the circuit. But actually I_0 flows down, because V_0 is measured with respect to ground.

$$\therefore \qquad A_v = \frac{-6.78}{0.2}$$

$$= -\ 33.9$$

Negative sign indicates that there is phase shift of 180^0 between input and output voltages, i.e. as base voltage goes more positive, (it is NPN transistor), the collector voltage goes more negative.

Example : 1.3

For the circuit shown, in Fig. (1.21), estimate A_v and R_i. $\frac{1}{h_{oe}}$ is large compared with the load seen by the transistor. All capacitors have negligible reactance at the test frequency.

h_{ie} = 1 kΩ, h_{fe} = 99 h_{re} is negligible.

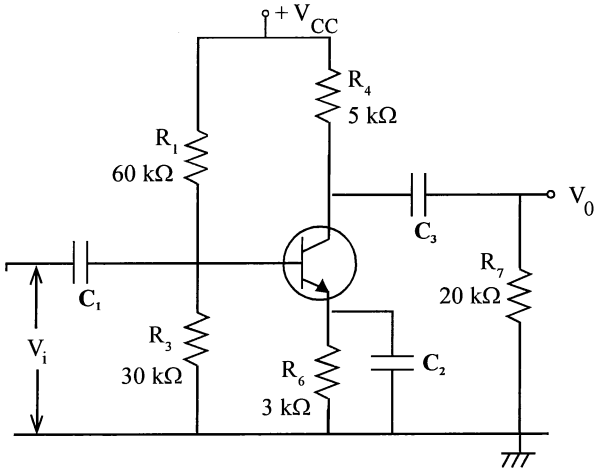

Fig. 1.21 AC amplifier circuit (Ex : 1.2)

Solution :

The same circuit can be redrawn as,

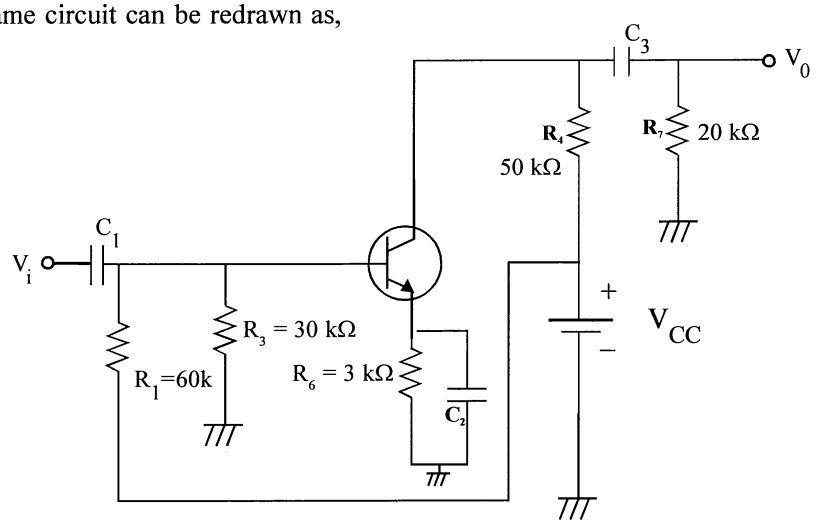

Fig. 1.22 Redrawn circuit of AC amplifier

In the second circuit also, R_4 is between collector and positive of V_{CC}. R_1 is between $+V_{CC}$ and base. Hence both the circuits are identical. Circuit in Fig. 1.21 is same as circuit in Fig. 1.22. In the AC equivalent circuit, the direct current source should be shorted to ground. Therefore, R_4 is between collector and ground and R_1 is between base and ground. Therefore, R_4 is in parallel with R_7 and R_1 is in parallel with R_3 (Fig. 1.23).

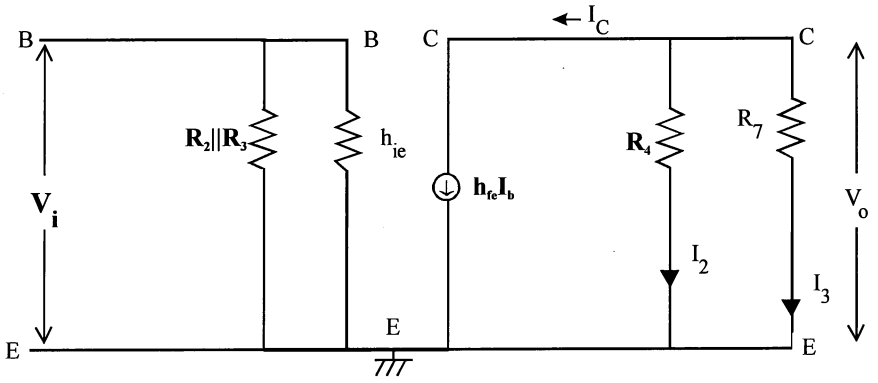

Fig. 1.23 h - Parameter equivalent circuit

$$R_2 \parallel R_3 = \frac{60 \times 30}{60 + 30} = \frac{1800}{90} = 20 \text{ k}\Omega.$$

$$R_4 \parallel R_7 = R_L = \frac{5 \times 20}{5 + 20} = 4 \text{ k}\Omega.$$

Therefore, the circuit reduces to, (as shown in Fig. 1.24).

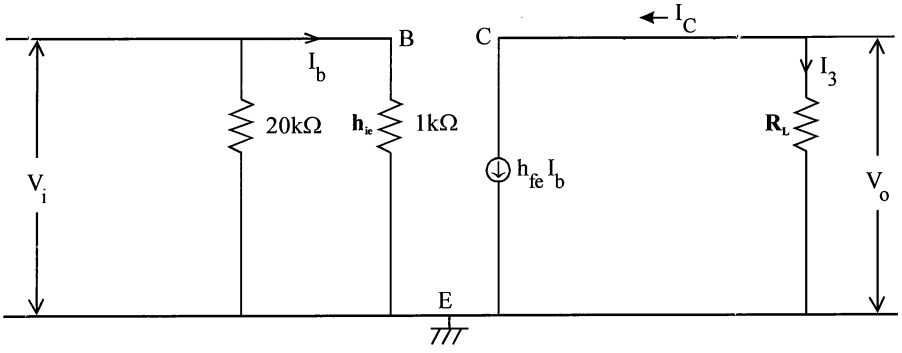

Fig. 1.24 Simplified circuit of Fig. 1.23

$$I_b = \frac{V_i}{h_{ie}} \qquad (\because h_{re} \text{ is negligible})$$

$$I_c = h_{fe} I_b = \frac{h_{fe} . V_i}{h_{ie}}$$

$$\therefore \quad V_0 = - I_c . R_L = - \frac{h_{fe} V_i . R_L}{h_{ie}}$$

$$A_v = \frac{V_0}{V_i} = - \frac{h_{fe} R_L}{h_{ie}} = \frac{-99 \ (14.28 \times 10^3)}{10^3}$$

$$A_v = -400$$

R_i is the parallel combination of 20 kΩ and h_{ie}.

$$\frac{20\times 1\ k\Omega}{20+1} = 950\ \Omega$$

Example : 1.4

Given a single stage transistor amplifier with *h - parameter* as h_{ic} = 1.1 kΩ, h_{rc} = 1, h_{fc} = –51, h_{oc} = 25 μA/v. Calculate A_I, A_V, A_{Vs}, R_i, and R_o for the Common Collector Configuration, with $R_s = R_L$ = 10 k.

Solution :

$$A_I = \frac{-h_{fc}}{(1+h_{oc}R_L)} = \frac{51}{1+25\times10^{-6}\times10^4} = 40.8$$

$$R_i = h_{ic} + h_{rc}A_I R_L = 1.1 \times 10^3 + 1 \times 40\ .\ 8 \times 10^4 = 409.1\ k\Omega$$

$$A_v = \frac{A_I.R_L}{R_i} = \frac{40.8\times10^4}{409.1\times10^3} = 0.998$$

$$A_{vs} = \frac{A_V \cdot R_i}{R_i + R_S} = \frac{0.998\times409.1}{419.1} = 0.974$$

$$R_0 = \frac{1}{h_{oc} - \frac{h_{fc}.h_{rc}}{h_{ic}+R_S}} = \frac{1}{25\times10^{-6} + \frac{51\times1}{(1.1+10)10^3}} = \frac{1}{4.625\times10^{-3}}$$

$$R_0 = 217\Omega$$

Example : 1.5

For any transistor amplifier prove that

$$R_i = \frac{h_i}{1-h_rA_V}$$

Solution :

$$R_i = h_i - \frac{h_f.h_r}{h_o + \frac{1}{R_L}}$$

But $$A_I = \frac{-h_f}{1+h_o.R_L}$$

$\therefore$ $$R_i = h_i + h_r A_I R_L \qquad .....(1.12)$$

$$\therefore \quad A_v = \frac{A_I . R_L}{R_i}$$

$$R_L = \frac{A_v . R_i}{A_I}$$

Substituting this value of R_L in equation (1.12)

$$R_i = h_i + \frac{h_r . A_I . A_V . R_i}{A_I} = h_i + h_r . A_V . R_i$$

$$R_i [1 - h_r A_v] = h_i \qquad \therefore \boxed{R_i = \frac{h_i}{1 - h_r A_v}}$$

Example : 1.6

For a Common Emitter Configuration, what is the maximum value of R_L for which R_1 differs by not more than 10% of its value at $R_2 = 0$?

$h_{ie} = 1100\ \Omega$; $h_{fe} = 50$

$h_{re} = 2.50 \times 10^{-4}$; $h_{oe} = 25\ \mu$ A/v

Solution :

Expression for R_i is,

$$R_i = h_{ie} - \frac{h_{fe} . h_{re}}{h_{oe} + \frac{1}{R_L}} .$$

If $R_2 = 0$, $R_i = h_{ie}$. The value of R_L for which $R_i = 0.9\ h_{ie}$ is found from the expression,

$$0.9\ h_{ie} = h_{ie} - \frac{h_{fe} . h_{re}}{h_{oe} + \frac{1}{R_L}}$$

or

$$\frac{h_{fe} . h_{re}}{h_{oe} + \frac{1}{R_L}} = h_{ie} - 0.9\ h_{ie} = 0.1\ h_{ie}$$

$$\frac{h_{fe} . h_{re}}{0.1 h_{ie}} = h_{oe} + \frac{1}{R_L}$$

$$\frac{1}{R_L} = \frac{h_{fe} . h_{re}}{0.1 h_{ie}} - h_{oe} = \frac{h_{fe}\ h_{re} - 0.1\ h_{oe}\ h_{re}}{0.1 h_{ie}}$$

or

$$R_L = \frac{0.1 h_{ie}}{h_{fe} h_{re} - 0.1 h_{oe}\ h_{ie}} = \frac{0.1 \times 1100}{50 \times 2.5 \times 10^{-4} - 0.1 \times 1100 \times 25 \times 10^{-6}}$$

$$R_L = 11.3\ \text{k}\Omega$$

1.4 MILLER'S THEOREM

Fig. 1.25(a) shows an amplifier with a capacitor between input and output terminals. It is called as feedback capacitor. When the gain K is large, the feedback will change the input Z and output Z of the circuit.

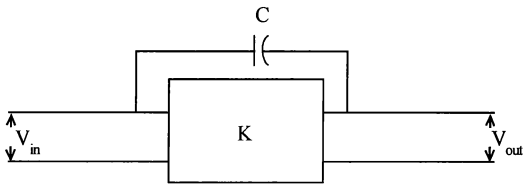

Fig. 1.25 (a) Feedback capacitor

A circuit as shown above is difficult to analyze, because of capacitor. So according to the Miller's theorem, the feedback capacitor can be split into two values, one as connected in the input side and the other on the output side, as shown in Fig. 1.25 (b).

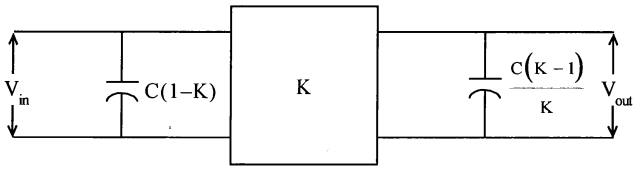

Fig. 1.25 (b) Splitting of feedback capacitor using Miller's theorem.

1.4.1 MATHEMATICAL PROOF OF MILLER'S THEOREM

The AC current passing through capacitor (C) in Fig. 1.25 (a) is

$$I_C = \frac{V_{in} - V_{out}}{\left(\frac{1}{j\omega c}\right)} = \frac{(V_{in} - V_{out})}{-J\,X_C}$$

$$V_{out} = K\,V_{in}$$

$$\therefore \quad I_C = \frac{(V_{in} - KV_{in})}{-jX_C} = \frac{V_{in}(1-K)}{-j\,X_C}$$

$$\frac{V_{in}}{I_C} = Z_{in} = \frac{V_{in}}{\frac{V_{in}(1-K)}{-jX_C}} = \frac{-jX_C}{(1-K)}$$

$$= \frac{-j}{2\pi f\,C(1-K)}$$

Since $$X_C = \frac{1}{2\pi f C}$$

$\frac{V_{in}}{I_C}$ is the input Z as seen from the input terminals.

$$\therefore \quad Z_{in} = \frac{-j}{2\pi f[C(1-K)]}$$

$$\therefore \quad C_{in} = C\ (1-K)$$

Similarly output capacitance can be derived as follows :

Current in the capacitor,

$$I_C = \frac{V_{out} - V_{in}}{-jX_C} = \frac{V_{out}\left(1 - \frac{V_{in}}{V_{out}}\right)}{-j\,X_C}$$

$$I_C = \frac{V_{out}\left(1 - \frac{1}{K}\right)}{-jX_C}$$

$$= \frac{V_{out}}{I_C} = Z_{out}$$

$$= \frac{V_{out}}{\frac{V_{out}\left(1 - \frac{1}{K}\right)}{-jX_C}}$$

$$Z_{out} = \frac{-jX_C}{\left(\frac{A-1}{A}\right)} = \frac{-j}{2\pi f C\left(\frac{K-1}{K}\right)}$$

$$\therefore \quad C_{out}\ (\text{Miller}) = C\left(\frac{K-1}{K}\right)$$

FREQUENCY EFFECTS

LEAD NETWORK (FIG. 1.26)

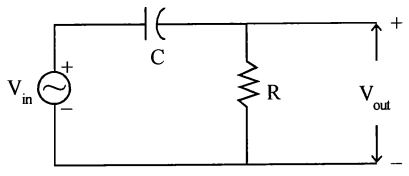

Fig. 1.26 Lead network

$$I = \frac{V_{in}}{R + \frac{1}{j\omega C}}$$

$$V_0 = I.\ R = \frac{V_{in}.R}{\left(R + \frac{1}{j\omega C}\right)}$$

V_0 leads with respect to V_{in}. So it is called as *lead network* for the above circuit (Fig. 1.25), at low frequencies, $X_C = \infty$.

$\therefore$ V_0 is low since (I is low). As f increases X_c decreases. Hence I flows, and V_o increases.

$\therefore$ Gain increases. Hence the frequency response is as shown.

Cut-off Frequency

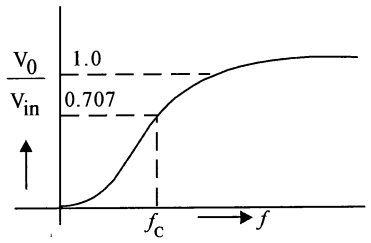

Fig. 1.27 Frequency response

$$V_{out} = \frac{R}{\sqrt{R^2 + X_C{}^2}}.V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{R}{\sqrt{R^2 + X_C^2}}$$

Cut-off frequency is the frequency at which $\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{2}}$.

This happens when, $X_c = R$

$$\frac{1}{2\pi f_c C} = R \quad \text{or} \quad \boxed{f_C = \frac{1}{2\pi RC}}$$

Lower cut-off frequency.

Half Power Point

At $f = f_C$, $P = \frac{V_{out}^2}{2R}$

Power is half of maximum power when V_{out} is maximum. Therefore it is also called as half power point.

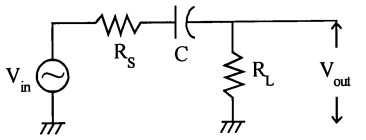

Fig. 1.28 Equivalent circuit

Considering Source Resistance :

$$\frac{V_{out}}{V_{in}} = \frac{R}{\sqrt{(R_S + R_L) + X_c^2}}$$

$$\text{At } f_C, \quad R_S + R_L = X_C$$

$$\therefore \quad f_C = \frac{1}{2\pi(R_S + R_L).C}$$

In the midband frequency region $X_C \cong 0$.

$$\therefore \quad \frac{V_{out}}{V_{in}} = \frac{R_L}{R_S + R_L}$$

$$A_{mid} \text{ (midband voltage gain)} = \frac{R_L}{R_S + R_L}$$

Stiff Coupling

If $X_c = 0.1\ (R_S + R_L)$ it is called *Stiff Coupling.*

The coupling capacitor must have (or bypass capacitor).

$$X_c = \frac{1}{10} R_E$$

This is known as *Stiff Coupling.*

Amplifier Analysis

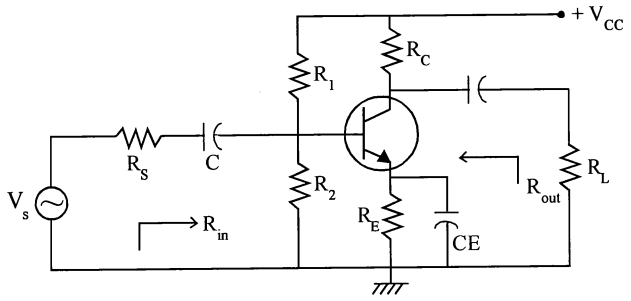

Fig. 1.29 Amplifier circuit

The equivalent circuit from input side, not considering R_S. (Fig. 1.30).
The equivalent circuit from output side, not considering R_L.

$$R_{in} = R_1 \parallel R_2 \parallel \beta r_e' \quad \text{(Not cosidering } R_S\text{)}$$
$$R_{out} \cong R_C \text{ (Not cosidering } R_L\text{)}$$

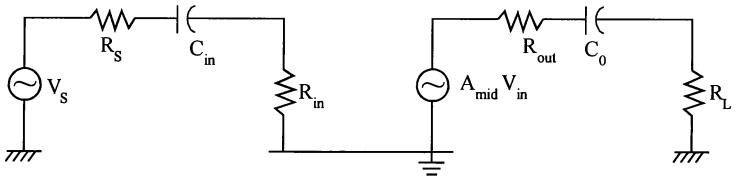

Fig. 1.30 Equivalent circuit

Considering the input side as a load network,

$$f_{in} = \frac{1}{2\pi(R_S + R_{in})C_{in}}$$

Similarly output lead network has cut-off frequency

$$f_{out} = \frac{1}{2\pi(R_{out} + R_L)C_{out}}$$

Lag Networks

$$V_0 = I.\, X_c$$
$$= \frac{V_i \,.\, X_C}{\left(R + \frac{1}{j\omega C}\right)}$$
$$V_0 = \frac{\frac{1}{j\omega C}.V_{in}}{\sqrt{R^2 + X_C{}^2}}$$
$$V_0 = \frac{-j(V_i/\omega C)}{\sqrt{R^2 + X_C^2}} \text{ therefore it is lag network}$$

V_0 lags with respect to V_i.

$$\frac{V_{out}}{V_{in}} = \frac{X_c}{\sqrt{R^2 + X_c{}^2}}$$

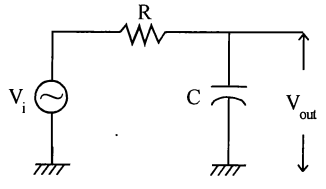

Fig. 1.31 Lag network

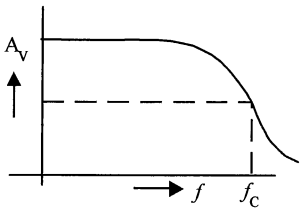

Fig. 1.32

at f_C, $R = X_C$

$\therefore$ $$\boxed{f_C = \frac{1}{2\pi RC}}$$

Midband gain $$A_{mid} = \frac{R_L}{R_S + R_L}$$

Decibel

Power gain = $G = \frac{P_2}{P_1}$

P_2 = Output power.

P_1 = Input power.

Decibel power gain = $G' = 10 \log_{10} G$.

If $G = 100$, $G' = 10 \log 100 =$ **20 db.**

If $G = 2$, $G' = 10 \log 2 = 3.01$db.

Usually, it is rounded off to 3.

Negative Decibel

If a < 1, a' will be negative.

If $G = \frac{1}{2}$,

$$G' = 10 \log \frac{1}{2} = -3.01 \text{ db}$$

	G	**G′**
If	1	0 db
	10	10 db
	100	20 db
	1000	30 db
	10, 000	40 db

Ordinary Gains Multiply :

If two stages are there,

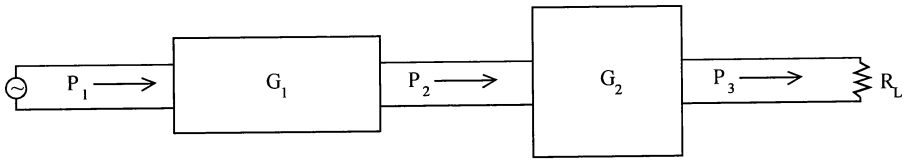

Fig. 1.33 Cascaded amplifier stages

$$G_1 = \frac{P_2}{P_1};\ G_2 = \frac{P_3}{P_2}$$

Overall gain $$G = \frac{P_3}{P_1}$$

$$= \frac{P_2}{P_1} \cdot \frac{P_3}{P_2}$$

$$\mathbf{G = G_1 G_2}$$

Decibel gains add up.

Decibel Voltage Gain

If A = Normal Voltage Gain $\frac{V_2}{V}$, decibel voltage gain $A' = 20 \log A$. $A = \frac{V_2}{V_1}$

If R_1 is output resistance,

Input power $$P_1 = \frac{V_1^2}{R_1}$$

If R_2 is output resistance, $P_2 = \frac{V_2^2}{R_2}$

$\therefore$ Power gain $$G = \frac{P_2}{P_1} = \frac{V_2^2}{V_1^2} \cdot \frac{R_1}{R_2}$$

If the impedances are matched, i.e. input resistance R_1 = output resistance R_2,

Power gain $$G = \frac{V_2^2}{V_1^2} = A^2$$

In decibels, 10 log $G = G' = 10 \log A^2$.

In decibels, 10 log $G = G' = 20 \log A$.

Cascaded Stages (Fig. 1.34)

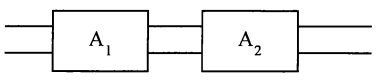

Fig. 1.34 Cascaded stages

$$A = A_1 \times A_2$$
$$A_1 = A_1' + A_2' \text{ (in decibels)}$$

Stiff Coupling

When the capacitor is chosen such that, $X_c = \frac{-R_E}{10}$, it is called as stiff coupling. Because, for the circuit shown.

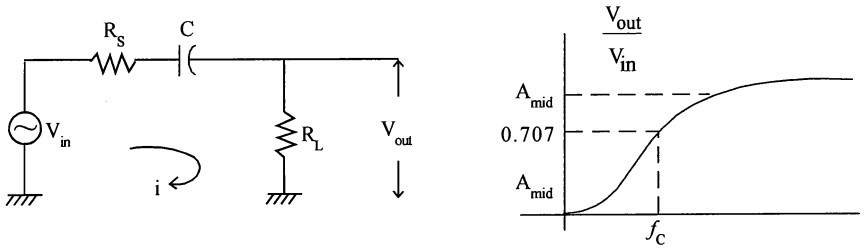

Fig. 1.35 Stiff coupling network

For the circuit, shown above, in the mid frequency range, X_c is negligible.

$$\therefore \quad i = \frac{V_{in}}{(R_S + R_L)}$$

$$V_{out} = i.\ R_L = \left(\frac{V_{in}}{R_S + R_L}\right) R_L.$$

$\therefore$ $A_{(mid)}$ = Voltage gain in the mid frequency range is,

$$A_{mid} = \frac{V_{out}}{V_{in}} = \frac{R_L}{R_S + R_L}$$

For the complete circuit, $\frac{V_{out}}{V_{in}} = \frac{R_L}{\sqrt{(R_S + R_L)^2 + X_c^2}}$

When $(R_S + R_L) = X_c, = \frac{1}{2\pi f_C C}$

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{\sqrt{2}(R_S + R_L)}$$
$$= 0.707\ A_{mid}$$

$$\therefore \quad f_C = \frac{1}{2\pi(R_S + R_L).C}$$

When $X_c = 0.1\ (R_S + R_L)$,

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{\sqrt{(R_S+R_L)^2+[0.1\,(R_S+R_L)]^2}}$$

$$\frac{V_{out}}{V_{in}} = 0.995\ A_{mid}.$$

X_c is made = 0.1 (R_S + R_L), at the lowest frequency. (f_C lower)

$\therefore$ At the frequency, A = 0.995 A_{mid}. So it is called as *Stiff Coupling*.

$$A = \frac{V_{out}}{V_{in}} = \frac{X_c}{\sqrt{R^2+X_c^2}} = \frac{1}{\sqrt{1+\left(\frac{R}{X_c}\right)^2}}$$

$\because$ $$\frac{R}{X_c} = \frac{R}{\frac{1}{2\pi f_C}} = 2\pi fRC = \frac{f}{f_C}$$

$\because$ $$f_c = \frac{1}{2\pi RC}$$

$\therefore$ $$A = \frac{1}{\sqrt{1+\left(\frac{f}{f_C}\right)^2}}$$

Decibel voltage gain $A' = 20 \log \frac{1}{\sqrt{1+\left(\frac{f}{f_c}\right)^2}}$

f_C = cutoff frequency.

When $\frac{f}{f_C} = 0.1$,

$$A' = 20 \log \frac{1}{\sqrt{1+(0.1)^2}} \cong 0\text{db}$$

When $\frac{f}{f_C} = 1$,

$$A' = 20 \log \frac{1}{\sqrt{1+1^2}} = -3.01\ \text{db} \cong 3\ \text{db}$$

When $\frac{f}{f_C} = 10$,

$$A' = 20 \log \frac{1}{\sqrt{1+10^2}} = -20 \text{ db}$$

When $\frac{f}{f_C} = 100$,

$$A' = 20 \log \frac{1}{\sqrt{1+100^2}} = -40 \text{ db}$$

When $\frac{f}{f_C} = 1000$,

$$A' = 20 \log \frac{1}{\sqrt{1+1000^2}} = 60 \text{ db}$$

$\therefore$ when $f = \frac{f_C}{10}$, $A' = 0$

$f = f_C$, $A' = -3$ db

$f = 10 f_C$, $A' = -20$ db

and so on.

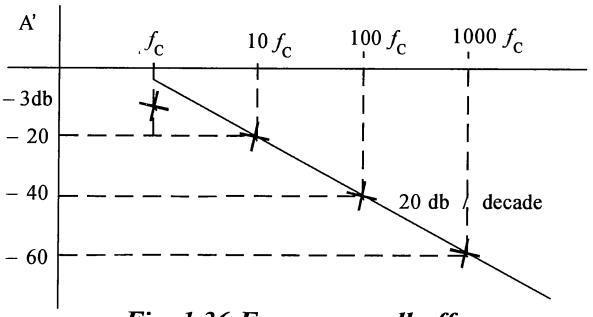

Fig. 1.36 Frequency roll-off

$\therefore$ A change of **20db** per decade *change* in frequency.

An Octave is a factor of 2 in frequency change

When *f changes from 100 to 200 Hzs, it has changed by one octave.*

When, *f* changes from 100 to 400 Hzs, it is two octaves for lead network, Bode Plot is

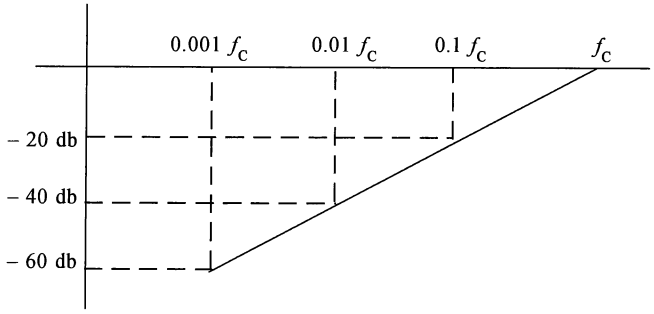

***Fig. 1.37 Variation of A_V with* f**

1.5 DESIGN OF SINGLE STAGE AMPLLIFIERS

To form transistor amplifier configuration, we connect a load impedance Z_L and a signal source as shown in Fig. 1.38.

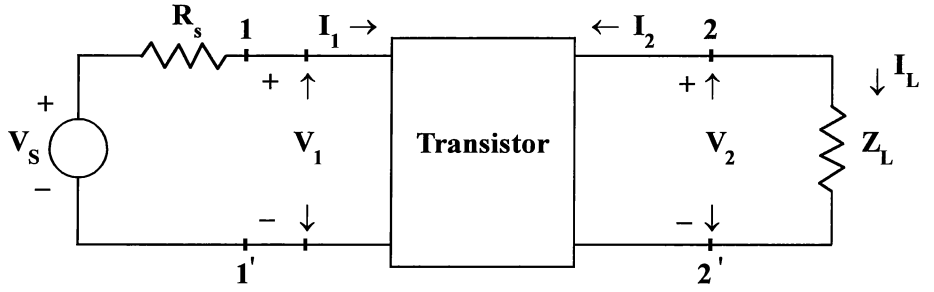

Fig 1.38 Amplifier circuit

V_s is the signal source, R_s is the resistance of the signal source, and Z_L is the load impedance. Transistor can be connected in C.E, C.B. and C.C. Configuration. To analyse these circuits i.e. to determine the current gain A_I, Voltage gain A_v, input impedance, output impedance etc, we can use the h parameters. So the equivalent circuit for the above transistor amplifier circuit in general form without indicating C.E, C.B, or C.C. Configuration, can be denoted as in the Fig. 1.39.

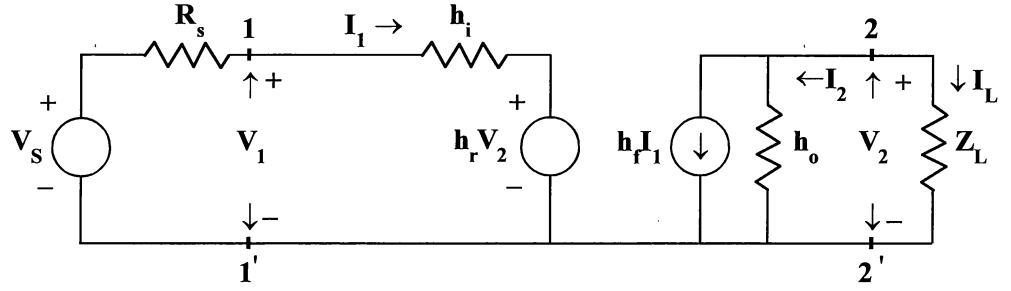

Fig 1.39 h-parameter equipvalent circuit (general repersentation)

Current Amplification,

$$A_I = \frac{I_L}{I_1};$$

But $I_L = -I_2$

$$\therefore \quad A_I = -\frac{I_2}{I_1};$$

Negative sign is because I_2 is always represented as flowing into the current source. For a transistor PNP or NPN type, if it is flowing out of the transistor, I_2 is represented as $-I_2$. Now voltage across Z_2 is taken with 2 as +ve and 2^1 as -ve The directions of I_L are as shown and $I_L = -I_2$.

From the above circuit we have,

$$I_2 = h_f I_1 + h_o V_2$$

But $V_2 = I_L Z_L = -I_2 . Z_L$ (Since $I_L = -I_2$)

$$\therefore \quad I_2 = h_f I_1 - h_o . Z_L . I_2$$

or $$I_2 + h_o Z_L I_2 = h_f I_1 .$$

$$I_2 (1 + h_o Z_L) = h_f I_1$$

$$\therefore \quad \boxed{A_I = - \frac{I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L}} \qquad \text{..... (1.13)}$$

Negative sign indicates that I_1 and I_2 are out of phase by 180^0.

1.5.1 Input Impedance (Z_i)

Input impedance of any circuit is the impedance we measure looking back into the amplifier circuit. Now amplifier terminals are 1and 1^1. R_s is the resistance of the signal source. So to determine the output z of the amplification alone, it need not be considered.

$$Z_i = \frac{V_1}{I_1}$$

But $$V_1 = h_i I_1 + h_r V_2 .$$

Hence $$Z_i = \frac{V_1}{I_1} = h_i + h_r . \frac{V_2}{I_1} . \qquad \text{..... (1.14)}$$

But $$V_2 = - I_2 . Z_L , \quad \therefore \frac{V_2}{I_1} = \left(\frac{-I_2}{I_1} \right) Z_L = A_I Z_L \qquad \text{..... (1.15)}$$

Substituting the values of V_2 in Equation (1.15),

$$\boxed{Z_i = h_i + h_r . A_I . Z_L}$$

But $$A_I = \frac{-h_f}{1 + h_o z_L}$$

$$\therefore \quad Z_i = h_i - \frac{h_f . h_r z_L}{1 + h_o z_L}$$

$$= h_i - \frac{h_f . h_r}{\frac{1}{z_L} + h_o}$$

$$\boxed{Z_i = h_i - \frac{h_f . h_r}{Y_L + h_o}} \qquad \text{..... (1.16)}$$

Y_L is load admittance. Therefore, Input impedance is a function of load impedance. If $Z_L = 0, Y_L = \infty$,

$$\therefore \quad Z_I = h_i .$$

1.5.2 Voltage Gain (A_V)

$$A_v = \frac{V_2}{V_1}$$

But $$V_2 = + I_L . Z_L = - I_2 . Z_L \qquad \text{Since, } I_2 = - I_L$$

But $I_2 = -A_I \cdot I_1$

$\therefore$ $V_2 = +A_I \cdot I_1 Z_L$.

$$\frac{v_2}{v_1} = \frac{A_I I_1 Z_L}{V_1}$$

But $$\frac{V_1}{I_1} = Z_i$$

$$z_i = h_i - \frac{h_f h_r}{\frac{1}{R_L} + h_o}$$

$\therefore$ $$A_V = \frac{A_I Z_L}{Z_i}$$

$$\boxed{A_V = -\frac{-h_f Z_L}{h_i + z_L(h_i h_o - h_f h_r)}} \quad \text{..... (1.17)}$$

1.5.3 Output Admittance (Y_o)

The output impedance can be determined by using two assumptions $Z_L = \infty$, and $V_s = 0$

Y_o is defined as $\frac{I_2}{V_2}$ with $Z_L = \infty$

But $I_2 = h_f I_1 + h_o v_2$.

Dividing by V_2,

$$\frac{I_2}{V_2} = Y_O = \frac{h_f I_1}{V_2} + h_o. \quad \text{..... (1.18)}$$

From the equivalent circuit with $V_s = 0$,

$$R_s \cdot I_1 + h_i I_1 + h_r V_2 = 0.$$

Dividing by V_2 Through out, we get

$$\frac{R_S \cdot I_1}{V_2} + \frac{h_i I_1}{V_2} + h_r = 0$$

or $$\frac{I_1}{V_2} = \frac{-h_r}{h_i + R_S} \quad \text{..... (1.19)}$$

Substitute this value in the equation for Y_o

$$Y_o = h_f \left(\frac{-h_r}{h_i + R_s}\right) + h_o$$

$$\boxed{Y_o = h_o - \frac{h_f . h_r}{h_i + R_s}}$$

Therefore, $Z_o = 1/Y_o$

Therefore, output admittance is a function of Source Resistance R_s where as Z_i is a function of Y_L. If $R_s = 0$, $Y_o \cong h_o$. Since ($h_f.h_r/h_i$) is very small.

1.5.4 Voltage Gain (A_{VS}) considering Source Resistance (R_S)

$$\therefore \quad A_{vs} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \times \frac{V_1}{V_S} = A_v . \frac{V_1}{V_S}.$$

This is the equivalent circuit of the input side of the amplifier circuit. (Fig. 1.40).

$$\therefore \quad V_1 = \frac{V_S . Z_i}{z_i + R_S}$$

$$\therefore \quad A_{vs} = \frac{A_V . Z_i}{Z_i + R_S}$$

$$A_v = \frac{v_2}{v_1}.$$

$$\therefore \quad A_V Z_i = \frac{V_2}{V_1} . Z_i$$

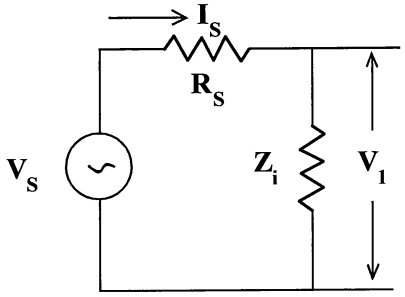

Fig 1.40 Voltage source.

But $V_2 = I_L . Z_L$; $V_1 = I_1 Z_i$

$$\therefore \quad A_v . z_i = \frac{I_L . Z_L . Z_i}{I_1 . Z_L} = A_I . Z_L$$

$$\therefore \quad \boxed{A_{vs} = \frac{A_L Z_L}{R_S + Z_i}.} \qquad \text{If } R_s = 0, A_{vs} = A_v . \qquad \text{..... (1.20)}$$

Hence A_V is the voltage gain of an ideal voltage source with zero terminal resistance.

1.5.5 Current Gain (A_{IS}) considering Source Resistance (R_S)

The input source can also be represented as a current source I_S in parallel with resistance R_s or voltage source V_s in series with resistance R_s. Now let us consider the input source as a current source in parallel with R_s. The equivalent circuit is (Fig. 1.41)

$$A_{IS} = \frac{I_L}{I_S} ; I_L = -I_2$$

$$\therefore \quad A_{IS} = \frac{I_L}{I_S} = -\frac{I_2}{I_S}$$

$$A_{IS} = -\frac{I_2}{I_S} = -\frac{I_2}{I_1} . \frac{I_1}{I_S}$$

$$= A_I . \frac{I_1}{I_S}$$

$$\therefore \quad A_I = \frac{-I_2}{I_1}.$$

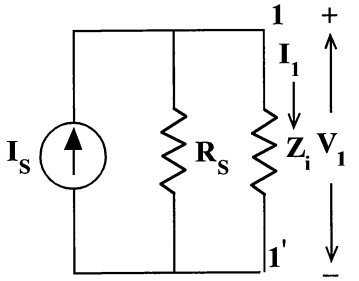

Fig 1.41 Current source

..... (1.21)

From the Fig 6.27, $I_1 = \dfrac{I_S.R_S}{R_S + Z_i}$

$$\therefore \quad A_{IS} = \frac{A_I \times R_S}{(R_S + Z_i)} = \frac{A_I.R_S}{(R_S + Z_i)}$$

If $R_S = \infty$, $A_I = A_{IS}$. Therefore, A_I is the current gain for an ideal source

Now $$A_{VS} = \frac{A_I.Z_L}{Z_i + R_s} \qquad \text{..... (1.22)}$$

$$A_{IS} = \frac{A_I.R_S}{Z_i + R_S} \qquad \text{..... (1.23)}$$

Dividing (1.10) and (1.11), $\dfrac{A_{vs}}{A_{IS}} = \dfrac{Z_L}{R_S}$.

or $$\boxed{A_{vs} = A_{IS}.\frac{Z_L}{R_S}} \qquad \text{..... (1.24)}$$

This equation is independent of the transistor parameters This is valid if the equivalent current and voltage sources have the same resistance.

1.5.6 Power Gain (A_P)

$$A_P = \frac{P_2}{P_1} = \frac{V_2 I_L}{V_1 I_1}$$

$$= A_v . A_I$$

$$\because \quad A_v = \frac{A_I.Z_L}{Z_i},$$

$$\therefore \quad \boxed{A_P = \frac{A_I^2 Z_L}{Z_i}} \qquad \text{..... (1.25)}$$

COMPARISON OF THE CE, CB, CC CONFIGURATIONS

C.E : Of the three, it is the most versatile. Its voltage and current gain are > 1. Input and output resistance vary least with R_s and R_L. R_i and R_o values lie between maximum and minimum for all the three configurations. Phase shift of 180^0 between V_i and V_o. Power Gain is Maximum.

C.B : $A_I < 1$ $A_V > 1$. R_i is the lowest and R_o is the highest . It has few applications. Sometimes it is used to match low impedance source V_i and V_o. No phase shift.

C.C : $A_V < 1$. A_I is very high. It has very ***high input Z and low output Z. So it is used as a buffer*** between high Z source and low impedance load. It is also called as ***emitter follower***.

To analyse circuit consisting of a number of Transistors, each Transistor should be replaced by its equivalent circuit in h-parameters. The emitter base and collector points are indicated and other circuit elements are connected without altering the circuit Configuration. This way the circuit analysis becomes easy.

Example 1.7

Find the Common Emitter Hybrid parameters in terms of the Common Collector Hybrid parameters for a given transistor.

Solution

We have to find h_{ie}, h_{re}, h_{fe} and h_{oe} in terms of h_{ic}, h_{rc}, h_{fc} and h_{oc}.

The transistor circuit in Common Collector Configuration is shown in Fig. 1.42. The h-parameter equivalent circuit is shown in Fig. 1.43.

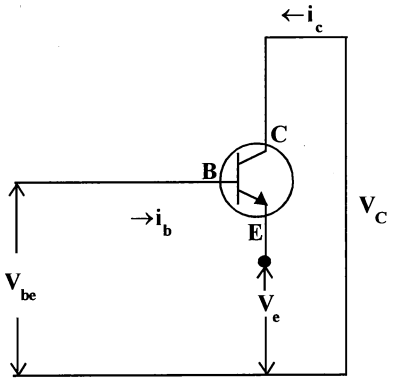

Fig 1.42 For example 1.7

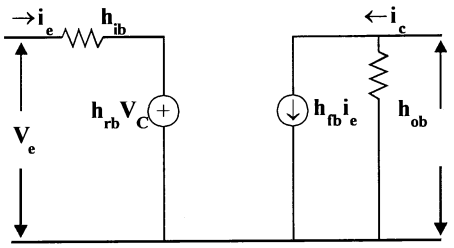

Fig 1.43 Equivalent circuit

C.C :

$$v_b = h_{ic}.\, i_b + h_{rC}\, v_e$$

$$i_e = h_{fc}\, i_b + h_{oC}\, v_e.$$

$$i_e = h_{fc}\, i_b - i_1$$

$$= (h_{fe}\, i_b - V_{ce}\, h_{oc})$$

$$v_{be} = i_b \,.\, h_{ic} - h_{rc}\, v_{ce} + v_{ce} = i_b \,.\, h_{ic} \qquad \text{Since } v_{ce} = 0$$

But $$h_{ie} = \left.\frac{V_{be}}{I_b}\right|_{V_{ce}=0}$$

$$\therefore \quad \boxed{h_{ie} = h_{ic}.} \qquad \text{..... (1.26)}$$

$$h_{fe} = \left.\frac{i_c}{i_b}\right| V_{ce} = 0$$

$$i_c = -i_b - i_e = -i_b - h_{fc} \,.\, i_b \,. + h_{oc}\, v_{ce}$$

But $v_{ce} = 0$

$$= -i_b - (h_{fc}\, i_b - h_{oc}\, v_{ce})$$

$$= -i_b - h_{fc}\, i_b + h_{oc}\, v_{ce} \qquad v_{ce} = 0$$

$$h_{fe} = \frac{-i_b - h_{fc} i_b}{i_b} = -(1 + h_{fc})$$

$$\boxed{h_{fe} = -(1 + h_{fc})} \qquad \text{..... (1.27)}$$

$$h_{re} = \frac{V_{be}}{V_{ce}}\Big|_{i_{b=0}}$$

$$V_{be} = i_b\, h_{ie} - h_{rc}\, V_{ce} + V_{ce}.$$

$$i_b = 0$$

$$\therefore \quad h_{re} = -\frac{h_{rc} v_{ce} + V_{ce}}{V_{ce}} = 1 - h_{rc}$$

$$\boxed{h_{re} = 1 - h_{rc}} \qquad \text{..... (1.28)}$$

$$h_{oe} = \frac{i_c}{V_{ce}}\Big| i_b = 0$$

$$i_c = -i_e - i_b$$

But $i_b = 0$.

$$i_c| = i_e$$

$$i_e = V_{ce}\, hoc$$

$$\therefore \quad \frac{i_e}{V_{ce}} = \frac{i_e}{V_{ce}} = h_{oc}$$

$$\therefore \quad i_c = -i_e = -h_{fc}\, i_b + V_{ce}\, h_{oc}$$

$$\therefore \quad \boxed{h_{oe} = h_{oc}} \qquad \text{..... (1.29)}$$

Since, $i_b = 0$

$$\therefore \quad i_c = V_{ce} \times h_{oc}$$

$$\therefore \quad h_{oe} = h_{oc}$$ is admittance in mhos (℧).

1.6 HIGH INPUT RESISTANCE TRANSISTOR CIRCUITS

In some applications the amplifier circuit will have to have very high input impedance. Common Collector Amplifier circuit has high input impedance and low output impedance. But its $A_V < 1$. If the input impedance of the amplifier circuit is to be only 500 kΩ or less the Common Collector Configuration can be used. This circuit is known as the ***Darlington Connection*** (named after Darlington) or ***Darlington Pair Circuit.*** (Fig. 1.44).

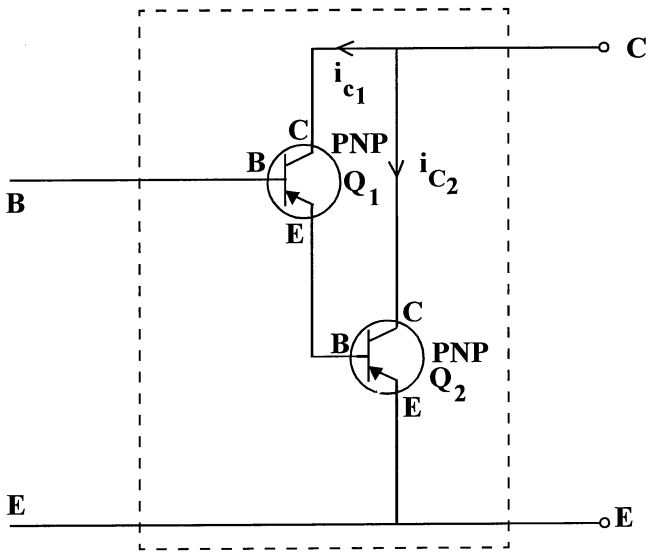

Fig 1.44 Darlington pair circuit.

In this circuit, the two transistors are in Common Collector Configuration. The output of the first transistor Q_1 (taken from the emitter of the Q_1) is the input to the second transistor Q_2 at the base. The input resistance of the second transistor constitutes the emitter load of the first transistor. So, Darlington Circuit is nothing but two transistors in Common Collector Configuration connected in series. The same circuit can be redrawn as AC equivalent circuit. So, DC is taken as ground shown in Fig.1.45. Hence, 'C' at ground potential. Collectors of transistors Q_1 and Q_2 are at ground potential. The AC equivalent Circuit is shown in Fig. 1.45.

There is no resistor connected between the emitter of Q_1 and ground i.e., Collector Point. So, we can assume that infinite resistance is connected between emitter and collector. For the analysis of the circuit, consider the equivalent circuit shown in Fig. 1.45 and we use Common Emitter ***h-parameters***, h_{ie}, h_{re}, h_{oe} and h_{fe}.

For PNP transistor, I_c leaves the transistor, I_e enters the transistor and I_b leaves the transistor.

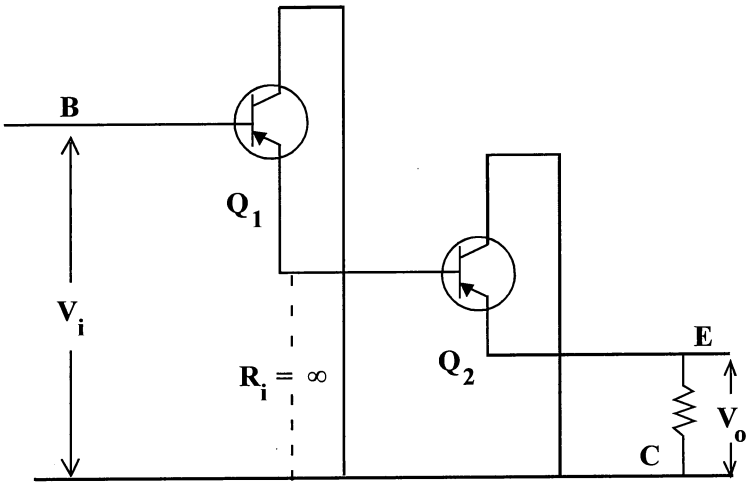

Fig 1.45 Equivalent circuit.

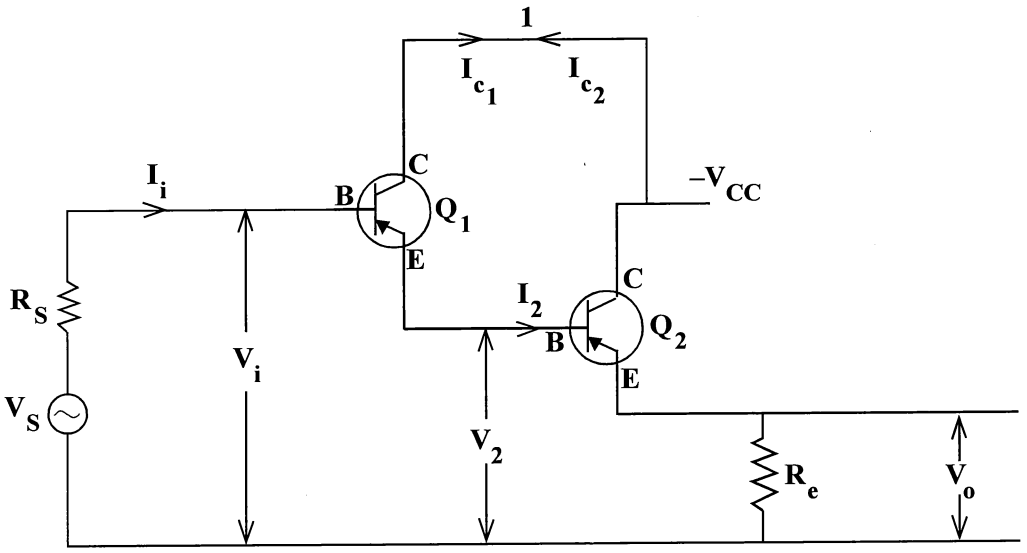

Fig 1.46 Darlington pair circuit.

1.6.1 Current Amplification For Darlington Pair

$$I_c = I_{c1} + I_{c2}.$$

$$I_{c1} = I_{b1}\, h_{fe};$$

$$I_{c_2} = I_{b_2}\, h_{fe}. \text{ (Assuming identical transistor and } h_{fe} \text{ is same)}$$

But $I_{b_2} = I_{e_1}$ (the emitter of Q_1 is connected to the base of Q_2)

$$\therefore \quad I_c = I_{b1} h_{fe} + I_{e1} h_{fe} \qquad \text{.....(1.30)}$$

$$I_{e_1} = I_{b_1} + I_{c_1} = I_{b_1}(1 + h_{fe}) \qquad \text{.....(1.31)}$$

$$\therefore \quad I_{c_1} = h_{fe}\, I_{b_1}$$

Substituting equation (1.31) in (1.30),

$$I_c = I_{b_1} h_{fe} + I_{b_1}(1 + h_{fe})h_{fe} = I_{b_1}(2h_{fe} + h_{fe}^2)$$

But $h^2_{fe} >> 2h_{fe}$

Since, h_{fe} is of the order of 100.

$$\therefore \quad I_c = I_{b_1} h_{fe}^2$$

It means that we get very large current amplification $\left(A_I = \frac{I_c}{I_{b_1}} \right)$, in the case of Darlington Pair Circuit, it is of the order h_{fe}^2 i.e. $100^2 = 10{,}000$.

$$\therefore \quad \boxed{A_I = \frac{I_c}{I_{b_1}} \cong (h_{fe})^2}$$

1.6.2 Input Resistance (R_i)

Input resistance R_{i_2} of the transistor Q_2 (which is in Common Collector Configuration) in terms of ***h- parameters*** in Common Emitter Configuration is,

$$R_{i_2} = h_{ie} + (1+h_{fe})\, R_L$$

But $h_{ie} << h_{fe}R_L$, and $h_{fe}\, R_E >> h_{ie}$ $A_{I_2} = \frac{I_0}{I_2} = (1 + h_{fe})$

Here R_L is R_e, since, output is taken across emitter resistance.

$$\therefore \quad Ri_2 \cong (1+ h_{fe})\, R_e$$

The input resistance Ri_1 of the transistor Q_1 is, since it is in Common Collector Configuration,

$$R_i = h_{ic} + h_{rc}\, A_I.R_L.$$

Expressing this in term of Common Emitter ***h-parameters***,

$$hic \cong h_{ie};\ h_{rc} \cong 1.$$

(For Common Collector Reverse Voltage Gain = 1) and R_L for transistor Q_1 is the input resistance of transistor Q_2.

$$\therefore \quad R_{i_1} = h_{ie} + A_{I_1}\, R_{i_2}.$$ R_{i_2} is large,

Therefore, $h_{oe}.R_{i_2} \leq 0.1$. and $A_I \# 1 + h_{fe}$

$$R_{i_1} \cong A_{I_1}\, R_{i_2}$$

$$R_{i_2} = (1 + h_{fe})\, R_e$$

But the expression for Common Collector Configuration in terms of Common Emitter ***h-parameters*** is

$$A_I = \frac{1+h_{fe}}{1+h_{oe}.R_L}$$

Here, $R_L = R_{i2}$ and $R_{i2} = (1 + h_{fe})\, R_e$.

$$\therefore \quad A_{I1} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe})R_e}$$

$h_{oe}\, R_e$ will be < 0.1 and can be neglected.

$$\therefore \quad h_{0e} \text{ value is of the order of } \mu \text{ mhos(micro mhos)}$$

$$\therefore \quad A_{I1} = \frac{1+h_{fe}}{1+h_{oe}h_{fe}R_e}$$

$$\therefore \quad R_{i1} \simeq A_{I1} \cdot R_{i2}$$

$$\boxed{R_i \simeq \frac{(1+h_{fe})^2 R_e}{1+h_{oe}h_{fe}R_e}}$$

This is a very high value. If we take typical values, of $R_e = 4\ k\Omega$, using ***h-parameters***,

$R_{i2} = 205\ k\Omega$.

$R_i = 1.73\ M\Omega$.

$A_I = 427$.

Therefore, Darlington Circuit has ***very high input impedance*** and very ***large current gain*** compared to Common Collector Configuration Circuit.

1.6.3 Voltage Gain (A_v)

General expression for A_v for Common Collector in term of ***h-parameters*** is

$$A_v = 1 - \frac{h_{ie}}{R_i};\ h_{ie} \cong h_{ic} \quad \text{or } A_{V1} = \frac{V_2}{V_i} = \left[\frac{1-h_{ie}}{R_{i1}}\right]$$

But $\quad R_i \cong A_{I1}.R_2. \quad \therefore A_{V1} = \left(-\frac{h_{ie}}{A_{I_1} R_{i2}}\right)$

$$\therefore \quad A_{V2} = \frac{V_o}{V_2} = \left(1 - \frac{h_{ie}}{R_{i_2}}\right)$$

Therefore, over all Voltage Gain $A_v = A_{v1} \times A_{v2}$

$$= \left(1 - \frac{h_{ie}}{A_{I_1}.R_{i_2}}\right)\left(1 - \frac{h_{ie}}{R_{i_2}}\right)$$

$$A_v \cong \left(1 - \frac{h_{ie}}{Ri_2}\right) \quad \because A_{I_1} R_{i2} >> h_{ie} \quad \because A_{i_1} \text{ is } >> 1$$

Therefore, A_v is always < 1.

1.6.4 Output Resistance (R_o)

The general expression for R_o of a transistor in Common Collector Configuration in terms of Common Emitter ***h-parameters*** is,

$$R_o = \frac{R_s + h_{ie}}{1+h_{fe}}$$

$$\therefore \quad R_{o1} = \frac{R_s + h_{ie}}{1+h_{fe}}$$

Now for the transistor Q_2, R_s is R_{o1}.

$$\therefore \qquad R_{o2} = \frac{\frac{R_S + h_{ie}}{1+h_{fe}}}{1+h_{fe}} + h_{ie}$$

Therefore, R_{o2} is the output resistance of the Darlington Circuit.

$$\therefore \qquad R_{o2} = \frac{R_s + h_{ie}}{(1+h_{fe})^2} + \frac{h_{ie}}{1+h_{fe}}$$

This is a small value, since, $1+ h_{fe}$ is >> 1.

Therefore, the characteristic of Darlington Circuit are

1. *Very High Input Resistance (of the order of MΩ).*
2. *Very Large Current Gain (of the order of 10, 000).*
3. *Very Low Output Resistance (of the order of few Ω).*
4. *Voltage Gain, A_v < 1.*

Darlington Pairs are available in a single package with just three leads, like one transistor in integrated form.

Disadvantages :

We have assumed that the ***h-parameters*** of both the transistor are identical. But in practice it is difficult to make out. ***h-parameters*** depend upon the operating point of Q_1 and Q_2. Since the emitter current of transistor Q_1 is the base current for transistor Q_2, the value of $I_{c2} >> I_{c1}$

1. *The quiescent or operating conditions of both the transistor will be different. h_{fe} value will be small for the transistor Q_1. $\because$ $h_{fe} = (I_c/I_b).I_{b2}$ is less*
   CDIL make CIL997 is a transistor of Darlington Pair Configuration with h_{fe} = 1000.
2. *The second drawback is leakage current of the 1st transistor Q_1 which is amplified by the second transistor Q_2 ($\because$ $I_{e1} = I_{b2}$).*
   Hence overall leakage current is more. Leakage Current is the current that flows in the circuit with no external bias voltages applied
   (a) *The **h-parameters** for both the transistors will not be the same.*
   (b) *Leakage Current is more.*
   (b) *Darlington transistor pairs in single package are available with h_{fe} as high as 30,000*

1.6.5 R-C Coupled Amplifier Circuit (Single Stage)

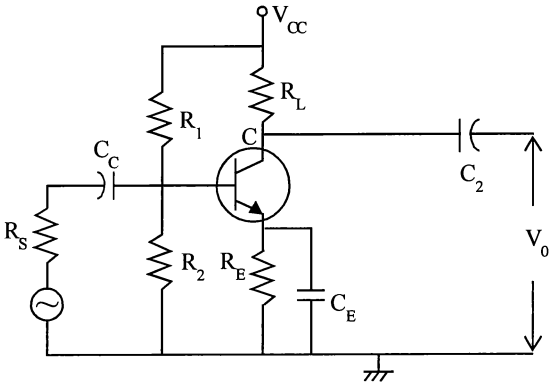

Fig. 1.47 RC Coupled amplifier circuit

The circuit is shown in Fig. 1.47.

R_L is the load resistor that develops the output voltage from the transistor. C_2 is used to couple the AC component of the output to R_L. (Fig. 1.47).

In the self bias circuit, R_E the emitter resistors is connected between emitter and ground. But through R_E, a negative feedback path is there. So to prevent A.C. negative feedback, if a capacitor is connected in parallel with R_E, and it is chosen such that X_E provides least resistance path compared to R_E, AC signal passes through C_E and not through R_E. Therefore, there will not be any negative feedback for AC signals.

$$X_E \text{ is chosen such that } X_E \leq \frac{R_E}{10}$$

and X_E is chosen at the frequency f_1. For frequencies higher than f_1, X_E any way will be less.

The equivalent circuit for the above transistor configuration is shown in Fig. 1.48.

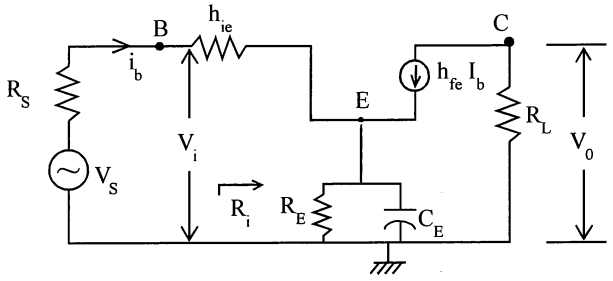

Fig. 1.48 Equivalent circuit

Suppose the value of C_C is very large. Then at the low and medium frequencies, the impedance is negligible. So the *equivalent* circuit is as shown. We shall consider the effect of C_E later.

From the *equivalent* circuit,

$$V_0 = - h_{fe} \cdot i_b \cdot R_L$$

negative sign is used since it is NPN transistor. The collector current is flowing into the transistor.

Input current, $I_b = V_s / R_s + R_i$

For a transistor amplifier circuit in common emitter configuration,

$$R_i = h_{ie} + (1 + h_{fe})\, Z_E.$$

Where $Z_E = R_E$ in parallel with $C_E = \dfrac{R_E}{1 + j\omega C_E R_E}$

$$\therefore \quad V_0 = -h_{fe}.\, R_L \times \frac{V_S}{R_S + h_{ie} + \dfrac{(1+h_{fe})R_E}{1 + j\omega C_E R_E}}$$

$$\therefore \quad A_V = \frac{V_0}{V_S}$$

A_V at low frequencies, (LF)

$$A_V(LF) = \frac{V_0}{V_S}$$

$$\boxed{A_V(LF) = \frac{-h_{fe}.\, R_L}{R_S + h_{ie} + \dfrac{(1+h_{fe})R_E}{1 + j\omega\, C_E R_E}}}$$

When ω is large, $\dfrac{(1+h_{fe})R_E}{1 + j\omega\, C_E R_E}$ can be neglected. So in the Mid Frequency range, (M.F.),

$$\therefore \quad \boxed{A_V(M.F) = \frac{-h_{fe} R_L}{R_S + h_{ie}}}$$

In this expression, there is no f or ω term. Hence in the mid frequency range, A_V is independent of f or the gain remains constant, irrespective of change in frequency.

1.6.6 Effect of Coupling Capacitor on Low Frequency Response

Consider the circuit shown in Fig. 1.49

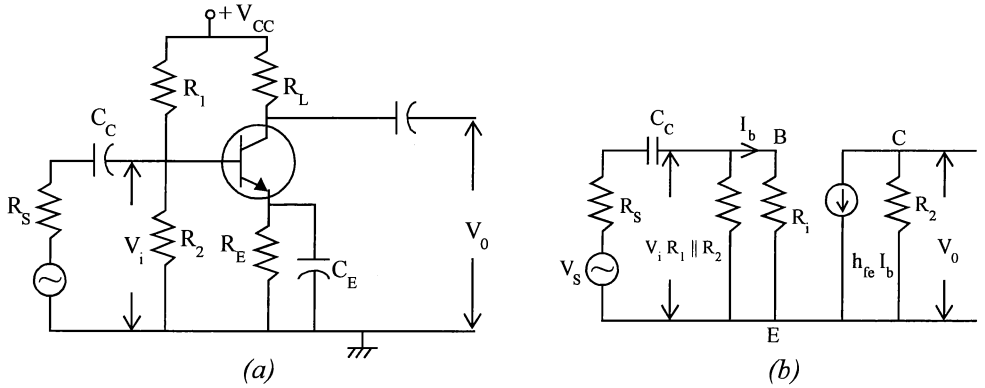

Fig. 1.49 Effect of coupling capacitors

Suppose that the value of C_E is such that its effect on the frequency response can be neglected and the value of X_C at low frequencies is such that it is not a simple short circuit for A.C. signals, so that its effect has to be considered.

The effect of C_E is, voltage drop across C_C will reduce V_i with a corresponding drop in V_0.

The frequency at which the gain drops by a factor of $\frac{1}{\sqrt{2}}$, is the lower 3 db frequency.

$$f_1 = \frac{1}{2\pi(R_S + R_i')C_C}$$

where $R_i' = R_1 \parallel R_2 \parallel R_i$

and $R_i = h_{ie}$, for an ideal capacitor C_E.

These expressions are valid when emitter is bypassed. In AC *equivalent circuit, emitter is assumed to be at GND potential. Therefore C_E has no effect.*

Large values of capacitors are required (10 μF, 5 μF etc.) in transistor amplifiers for coupling and bypass purposes for good low frequency response. Since these values are large, only electrolytic capacitors are used. Capacitors of such large values are not available in other types of capacitors. These capacitors are bulky. So audio amplifier circuits, Integrated Circuits (I.C) often have large capacitors connected externally to the (I.C) itself to provide the required low frequency response.

Example : 1.8

In the Resistance Capacitance (RC) coupled amplifier, $A_{v_m} = 50$, $f_1 = 50$ Hz and $f_2 = 100$ kHz. Find the values of frequencies at which the gain reduces to 40 on either side of midband region.

Solution :

$$A_{VH} = \frac{A_{V\,MF}}{1 + j\left(\frac{f}{f_2}\right)}$$

Phase shift angle $\phi = 180^\circ - \tan^{-1}\left(\frac{f}{f_2}\right)$

$$A_{V\,LF} = \frac{A_{V\,MF}}{\sqrt{1 + \left(\frac{f_1}{f}\right)^2}}$$

$$A_{VL} = \frac{A_{VM}}{1 + j\left(\frac{f_1}{f}\right)}$$

$$\phi = 180^o + \tan^{-1}\left(\frac{f_1}{f}\right)$$

At the frequency f, the gain is $A_{V\,L.F} = 40$.

$A_{VL.F} = 40$, $A_{VM..F} = 50$, $f_1 = 50$ Hzs, $f = ?$

$$\frac{40}{50} = \frac{1}{\sqrt{1 + \left(\frac{50}{f}\right)^2}} \qquad \therefore f = 66.66 \text{ Hz.}$$

$$A_{V\,H.F} = \frac{A_{V\,M.F}}{\sqrt{1 + \left(\frac{f}{f_2}\right)^2}}$$

At frequency f, $A_{V\,H.F} = 40$. $\therefore$ $f = ?$ $f_2 = 100$ kHz.

$$\frac{40}{50} = \frac{1}{\sqrt{1 + \left(\frac{f}{100 \times 10^3}\right)^2}}; \qquad f = 75 \text{ kHz.}$$

Example : 1.9

An amplifier of 40db gain has both its input and output load resistances equal to 600Ω. If the amplifier input power is – 30db, what is the output power and voltage ? Assume that reference power level used is 1mW in a 600 Ω resistance.

Solution :

Since it is logarithmic scale, for dbs,

P_0 (db) = $(P_i)_{db}$ + (gain $_{db}$);

$P_0 = P_i \times A_P$ Output power (P_0) = Input Power (P_i) × Power Gain (A_P)

$P_0 = ? P_i = -30$db, gain = 40db

$\therefore$ $P_0 = -30 + 40 =$ **10db.**

Reference power level = 1 mW.

$$\therefore \quad 10 \log = \left(\frac{P_0}{1mW}\right) = 10db$$

$$10 \log \frac{P_0}{0.001} = 10$$

$$\log \frac{P_0}{0.001} = 1$$

$$\frac{P_0}{0.001} = 10$$

$\because$ $\log 10 = 1$

$\therefore$ $P_0 = 10 \times 0.001$

$= \mathbf{10mW}$

(With respect to, 1mW, the input and output powers are compared and expressed in db.

$$\therefore \quad 10 \log \frac{P_0}{1mW} = 10db)$$

RMS output voltage is,

$$P_0 = \frac{V_0^2}{R}$$

or $$V_0 = \sqrt{P_0.R} = \sqrt{10 \times 10^{-3} \times 600}$$

$= \sqrt{6} = \mathbf{2.45\ V}$

Example : 1.10

An amplifier has $R_i = 0.5\ k\Omega$ and $R_0 = 0.05\ k\Omega$. The amplifier gives an output voltage of 1V peak for an input voltage of 1mV peak. Find A_V, A_i, A_P in db.

Solution :

V_0 (peak) = 1V.

$$V_{0\ (rms)} = \frac{V_0(peak)}{\sqrt{2}}; \qquad V_{0\ (rms)} = \frac{1V}{\sqrt{2}}$$

$$A_V = 20 \log \left(\frac{V_0}{V_i}\right)$$

$$= 20 \log \left(\frac{1}{1mV} \right) = 60 \text{ db}$$

$$I_{i\,(peak)} = V_{i\,(Peak)} / R_i$$
$$= 1mV/500$$
$$= 2 \times 10^{-6} \text{ A.}$$
$$I_{0\,(peak)} = V_{0\,(Peak)} / R_0$$
$$= 1/50$$
$$I_{0\,(Peak)} = 0.02 \text{ A.}$$

$\therefore$ Current Gain $(A_i) = 20 \log \left(\frac{0.02}{2 \times 10^{-6}} \right) =$ **80 db**

$$P_i = \frac{V_i^2}{R_i} = 10^{-9} \text{ W;}$$

$$P_0 = \frac{V_0^2}{R_0} = 10^{-2} \text{ W.}$$

Power gain, $A_P = 10 \log \left(\frac{P_0}{P_i} \right) =$ **70 db**

SUMMARY

- Electronic amplifiers are classified based on (a) Frequency range (b) Type of coupling (c) Output power (d) Type of signal handled.
- Power amplifiers are classfied as (a) Class A (b) Class B (c) Class AB (d) Class C (e) Class D and (f) Class S amplifiers.
- The type of distortion that can occur are classified as (a) amplitude (b) frequency (c) Phase distrotions
- h-parameter analysis enables to derive expressions for A_I, A_v, R_i, R_o, A_p of amplifiers in terms of transistor parameters and circuit components. These equations are derived.
- Gain is expressed in decibles.
- Comparison between the three types, C.E, CB, CC amplifiers is given and expressions are derived for A_I, A_V, Z_i, Z_0, A_p etc.
- Darlington pair amplifier circuit gives high R_i (MΩ) large current gain (10K), low voltage gain (<1) and low R_0 (few Ω). The circuit is explained and equations are derived.
- Single stage R-C coupled amplifier circuit is given and expressions for lower cut-off frequency and upper cut-off frequency are given.

OBJECTIVE TYPE QUESTIONS

1. The units of h-parameters are .....
2. h-parameters are named as hybrid parameters because .....
3. The general equations governing h-parameters are

   V_1 = ...

   I_2 = ...
4. The parameter h_{re} is defined as h_{re} = ...
5. h-parameters are valid in the ..... frequency range.
6. Typical values of h-parameters in Common Emitter Configuration are .....
7. The units of the parameter h_{rc} are .....
8. Conversion Efficiency of an amplifier circuit is .....
9. Expression for current gain A_I in terms of h_{fe} and h_{re} are A_I = ...
10. In Common Collector Configuration, the values of $h_{rc} \simeq$ .....
11. In the case of transistor in Common Emitter Configuration, as R_L increases, R_i .....
12. Current Gain A_I of BJT in Common Emitter Configuration is high when R_L is ..... .
13. Power Gain of Common Emitter Transistor amplifier is ..... .
14. Current Gain A_I in Common Base Configuration is ..... .
15. Among the three transistor amplifier configurations, large output resistance is in ..... configuration.
16. Highest current gain, under identical conditions is obtained in ..... transistor amplifier configuraiton.
17. C.C Configuration is also known as ..... circuit.

ESSAY TYPE QUESTIONS

1. Write the general equations in terms of h-parameters for a BJT in Common Base Amplifiers configuration and define the h-parameters.
2. Convert the h-parameters in Common Base Configuration to Common Emitter Configuration, deriving the necessary equations.
3. Compare the transistor (BJT) amplifiers circuits in the three configurations with the help of h-parameters values.
4. Draw the h-parameter equivalent circuits for Transistor amplifiers in the three configurations.
5. With the help of necessary equations, discuss the variations of A_V, A_I, R_i R_O, A_P with R_S and R_L in Common Emitter Configuration.
6. Discuss the Transistor Amplifier characteristics in Common Base Configuration and their variation with R_S and R_L with the help of equations.
7. Compare the characteristics of Transistor Amplifiers in the three configurations.

ANSWERS OF OBJECTIVE TYPE QUESTIONS

1. Ω, mhos and constants
2. the units of different parameters are not the same
3. $h_{11}I_1 + h_{12}V_2$
   $h_{21}I_1 + h_{22}V_2$
4. $\left.\frac{\partial V_B}{\partial V_C}\right|_{I_B=K}$
5. Audio
6. $h_{ie} = 1\ k\Omega$, $h_{re} = 1.5 \times 10^{-4}$,
   $h_{oe} = 6\mu mhos$, $h_{fe} = 200$
7. No units (constant)
8. $\frac{\text{AC Signal Power Delivered to the Load}}{\text{DC Input Power}} \times 100$
9. $\frac{h_{fe}}{1 + h_{oe}R_L}$
10. 1
11. Decreases
12. Low
13. Large
14. < 1
15. Common Base configuration
16. Common Collector Configuration
17. Voltatge follower/buffer